Thermal Modeling of Ultraviolet Nanoimprint Lithography

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Nanoimprint lithography (NIL) is a promising nanomanufacturing technology that offers an alternative to traditional photolithography for manufacturing next-generation semiconductor devices. This technology involves coating an ultraviolet (UV)-curable monomer layer on the substrate and then imprinting it with a template containing topography corresponding to the desired substrate features. While the template is close to contact with the substrate, the monomer is cured by UV exposure. This results in definition of desired features on the substrate. While NIL has the potential of defining very small feature sizes, thermal management of this process is critical for ensuring accuracy. Heat generation in the monomer layer due to UV absorption needs to be managed and dissipated in order to avoid thermal expansion mismatch and consequent misalignment between the template and wafer. In addition, thermal dissipation must occur in a timeframe that does not adversely affect the required lithography throughout. This paper develops a numerical simulation model of the nanoimprinting process and utilizes the model to study the effect of various geometrical parameters on the accuracy and throughput of the process. The effect of the UV power characteristics on heat dissipation and consequently on misalignment due to thermal expansion is studied. Results indicate that the thermal expansion mismatch due to commonly used UV exposure parameters may be minimized by utilizing a lower exposure power for longer time. A transient model enables a study of the effect of die imprint sequencing on the overall temperature rise during the process. Results indicate a critical trade-off between minimizing temperature rise on one hand, and maximizing system-level throughput on the other. By identifying and quantifying this trade-off, this work contributes to development of error-free nanoimprint lithography for future technology nodes. [DOI: 10.1115/1.4025564]

Keywords: nanoimprint lithography, nanomanufacturing, semiconductor nanofabrication, thermal management

1 Introduction

NIL [1,2] has emerged as a promising technology for scalable nanomanufacturing of nanoscale features for semiconductors and a variety of other applications [3–5]. The underlying basis of this technology is the transfer of a pattern from a master template to a substrate. NIL encompasses a variety of means for the pattern transfer. The most common technique, shown schematically in Fig. 1, involves spinning a UV-curable monomer on the substrate, aligning and pressing down the master template, followed by UV exposure through the template, typically at a wavelength of around 390 nm [1]. By doing so, monomer trapped in the topography of the template cures and hardens. The template surface and monomer are engineered such that the template can be removed without tearing the hardened monomer, which retains the pattern of the template [6]. It has been shown that NIL is capable of high throughput manufacturing of nanoscale features on large areas. Pattern accuracy achieved by NIL is comparable to other competing technologies for nanofabrication [3]. The relatively lower cost of nanoimprinting compared to deep ultraviolet (deep-UV) lithography has established NIL as a contender for next-generation lithography solution for semiconductor devices [3]. Besides transistor-based semiconductor devices, NIL has also been demonstrated for several other applications for which scalable nanomanufacturing is critical. This includes semiconductor memory devices [7], solar cells [8], etc. In addition to nanoimprinting on rigid substrates, roll-to-roll nanoimprinting has also been demonstrated [4].

There are several challenges in maintaining and improving NIL pattern accuracy. It is important to understand and model the mechanics of template removal from the substrate following UV exposure [6]. Challenges arising from mechanical rigidity of the template have been met by designing and implementing flexible templates [9,10]. On the other hand, several thermal effects in nanoimprinting have not been investigated in much detail. While the substrate is exposed to UV radiation for curing the monomer, an inadvertent side effect of this process is heat diffusion into the substrate, due to which the substrate temperature rises. This thermal effect may severely limit the capability of nanoimprinting due to misalignment caused by uneven thermal expansion of the substrate and template [11]. When the alignment requirement is of the order of tens of nanometers or lower, a temperature rise of even a fraction of 1 °C is sufficient to cause process failure. Further, the generation of thermomechanical stresses due to uneven thermal expansion may cause undesirable effects such as warpage, residual stresses and reduced transistor performance [12]. Finally, heat absorption in the monomer may cause changes in its properties, which may affect its curing chemistry [13]. Thus, temperature rise during the UV exposure process must be kept at a minimum. While several other technological challenges for enabling NIL have been addressed, relatively lesser work has been carried out on the understanding and modeling of temperature rise and consequent thermal expansion mismatch in NIL. Heating effects due to UV exposure need to be fully understood and modeled. Thermal analysis for step-and-imprint NIL has been carried out, and the temperature rise for single and multiple imprints in vinyl ether monomer has been predicted [13]. Modeling of laser absorbance and heating during laser-assisted direct nanoimprint processing has been carried out [14]. Placement error due to thermal expansion mismatch has been investigated experimentally [15]. While this work does not include any thermal modeling, it does suggest that thermal expansion mismatch related pattern distortion in NIL may be a significant concern. Some work has been reported on compensation of thermal expansion mismatch by Moiré fringe techniques [16]. While this results in significant overlay improvement, it would be preferable to develop smart thermal management techniques that minimize the temperature rise during the UV exposure process, which is the underlying reason for overlay mismatch. A fundamental study of thermal effects in manufacturing processes based on nanoimprinting will lead to a better understanding of process limitations due to thermal effects, and will help develop novel design tools to mitigate such effects.

In this paper, thermal modeling of the nanoimprint process has been carried out in order to develop a fundamental understanding of thermal transport during the nanoimprinting process. Finite-element simulations are carried out to characterize temperature rise during a single-field imprint as a function of UV power and exposure duration. Thermomechanical stress generation in the substrate is also analyzed as a function of various heating power densities. A sequential multifield exposure process is analyzed, and trade-offs between temperature rise and throughput speed are identified. Results obtained from these simulations are expected to help in designing thermal-friendly techniques for error-free nanoimprint lithography at current and future technology nodes.

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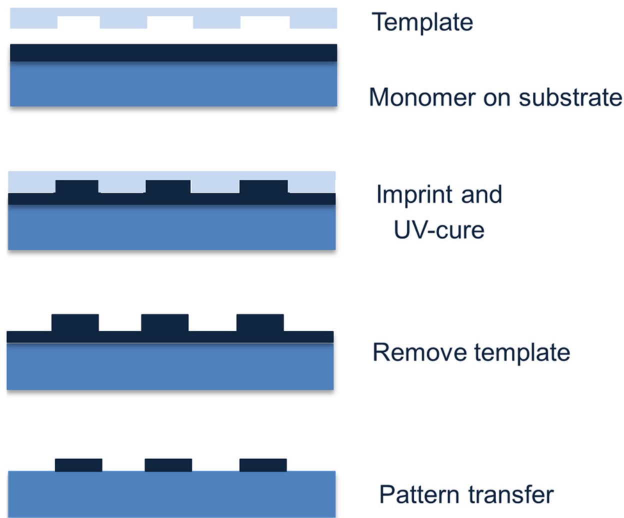

Fig. 1 Schematic of the nanoimprinting process

2 Heat Transfer During Nanoimprint Process

Figure 2 shows a schematic of the geometry of the nanoimprinting process. Instead of nanoimprinting the entire substrate wafer, it is usually divided into a number of fields on which the UV-curable monomer is dispersed, followed by UV exposure and cure, usually at a UV wavelength of 390 nm [1]. The substrate wafer is supported on a wafer chuck, usually through vacuum holes. Similarly, the template is supported on a template chuck. The entire system is usually cooled from the wafer chuck backside using liquid cooling. Some heat dissipation also occurs through the backside of the template chuck. The three-dimensional governing energy conservation equation in this case is given by

$$k\left[\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}\right]+Q(x,y,z)=\rho C_p\frac{\partial T}{\partial t} \tag{1}$$

where $T(x,y,z,t)$ is the temperature rise over ambient; k, ρ, and C_p are thermal conductivity, density, and heat capacity of the respective material, and $Q(x,y,z)$ is the heat generation rate due to absorption from the UV source.

Boundary conditions at the backside of the wafer chuck and template chuck are given by

$$-k_i\frac{\partial T}{\partial \bar{n}_i}=h_i T \tag{2}$$

where the subscript i refers to either the wafer chuck or template chuck, h_i refers to the convective heat transfer coefficient, and $\bar{n}_i$ is the outward normal at the ith surface.

An adiabatic boundary condition is assumed on all other surfaces. Finally, it is assumed that the initial temperature rise is zero throughout the entire geometry.

In order to understand the thermal dynamics of this system, a three-dimensional finite-element model of the entire geometry is developed in ANSYS CFX. UV irradiance of the exposed field due to UV irradiance is modeled as volumetric heat generation in the thin monomer film on top of the field of the substrate which is being developed. It is assumed that the entire UV power irradiated on the monomer is absorbed by the monomer, resulting in volumetric heat generation. It is well-known that incident UV irradiance is absorbed primarily by the monomer film, whereas the template material through which the UV radiation passes prior to reaching the monomer, absorbs negligible UV irradiance [13]. Further, while polymerization is typically an exothermic reaction, the heat of reaction for commonly used acrylate and vinyl ether monomers is around 500 kJ/kg [17–19], which for a typical 10 mm by 10 mm field size results in negligible heat generation. Finally, the net heat absorption during photoinitiation processes underlying polymerization is found to be negligible compared to incident radiation, based on the UV wavelength. In any case, since photoinitiation absorbs energy, it is a good conservative assumption to neglect this heat absoption. Wafer chuck backside cooling, usually carried out by passing a liquid coolant through the wafer chuck backside is modeled using a prescribed heat transfer

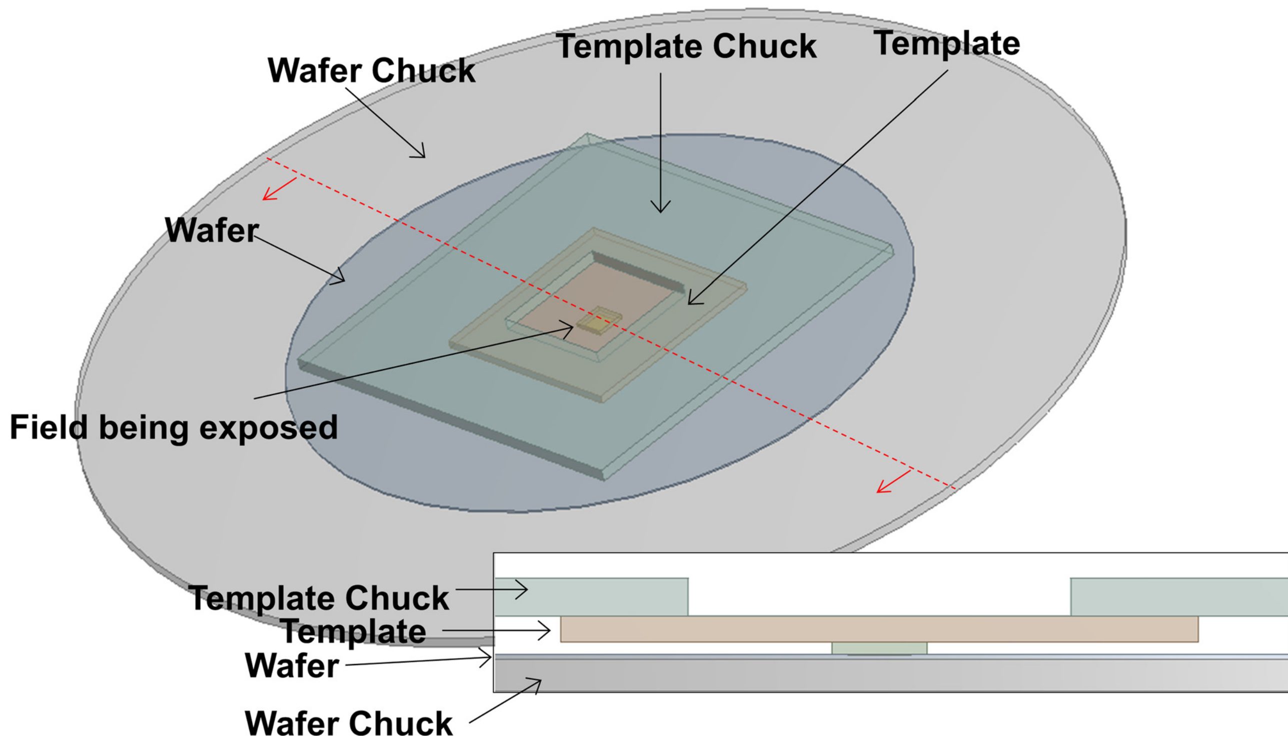

Fig. 2 Schematic of the geometry of UV exposure and development process during nanoimprinting

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Table 1 **Thermal and thermomechanical properties of various materials in the model. Property values taken from Ref. [19].**

Material	Thermal conductivity (W/m K)	Heat capacity (J/Kg K)	Density (kg/m^3)	Young's modulus (MPa)	Poisson's ratio	CTE (K^{-1})
Cooper	401	3.85	8960	1.15×10^5	0.34	1.65×10^{-5}
Silicon	148	0.7	2.33	1.5×10^5	0.17	2.6×10^{-6}
Silica	1.38	740	2.65	7.3×10^4	0.17	5.5×10^{-7}
Aluminum	237	903	2.702	7×10^4	0.35	2.31×10^{-5}

coefficient of 5000 W/m^{2}K. The heat transfer coefficient on the template chuck backside is assumed to be 1000 W/m^{2}K, which is representative of air cooling. A 300 mm diameter wafer is assumed. The size of the field being exposed is assumed to be 10 mm by 10 mm, which is a typical microprocessor size. The material for wafer, wafer chuck, template and template chuck are assumed to be silicon, aluminum, silica and aluminum, respectively. The diameters of the wafer and wafer chuck are assumed to be 300 mm and 500 mm, respectively, based on standard sizes used in nanomanufacturing. The thicknesses of the wafer and wafer chuck are assumed to be 0.8 mm and 4.5 mm, respectively. The size of the template and template chuck are assumed to be 60 mm by 60 mm by 6 mm and 15 mm by 15 mm by 2 mm, respectively. Standard thermal properties of each constituent material is used [19], as summarized in Table 1. Since the temperature range in these simulations is somewhat small, it is reasonable to assume that these properties do not change significantly with temperature. By doing so, a transient thermal simulation model is developed. Grid refinement testing is carried out to ensure that results are grid independent. All results presented in this paper are obtained with around 600 K nodes. Figure 3 shows a cross-section temperature plot indicating the temperature distribution due to the nanoimprint lithography process. The plot shows, as expected, the maximum temperature to occur at the site of the field being exposed.

It is found that the peak transient temperature during the UV exposure process is not affected by the wafer chuck backside cooling characteristics. This is because at an exposure time of the order of hundreds of ms, the thermal penetration depth is of the order of a few mm, which is smaller than the combined wafer and wafer chuck thicknesses. The wafer chuck itself is usually tens of mm thick due to vacuum and coolant lines within the chuck. As a result, the peak temperature at the end of the exposure process remains unaffected by the cooling conditions on the wafer chuck backside.

The temperature field during nanoimprinting is transient, because the exposure time is typically greater than the time it takes for the temperature field to reach steady-state in response to the imposed heat generation due to UV exposure. Based on the monomer polymerization chemistry, a fixed energy needs to be transferred to the monomer per unit area. As a result, a critical thermal design problem for UV exposure is to determine how much power density to expose at. Based on the magnitude of the power density, the total exposure time may be determined. Figure 4 shows a plot of the maximum temperature for a number of power density values, for the same total energy density of 300 mJ/cm^2 being transferred to the monomer. For this plot, the field being exposed is assumed to be 10 mm by 10 mm, a typical microprocessor size. The wafer diameter and thickness are assumed to be 300 mm and 0.8 mm, respectively, both of which are typical of semiconductor device wafers. The field being exposed is assumed to be located in the center of the wafer. Note that as the power density increases, the required exposure time reduces for constant total energy density. In this case, the exposure time varies from 30 s to 0.3 s. This plot clearly shows that the higher the power density, the higher is the temperature rise. As a result, a low power density dosage for a longer time is thermally preferable. The result obtained in Fig. 4 makes intuitive sense, since the longer the exposure process, the easier it is for heat to diffuse from the field being exposed to adjacent fields on the substrate wafer. As a result, for the same total exposure, it is thermally preferable to expose with a lower power density and higher exposure time.

While the temperature rise shown in Fig. 4 may appear to be of somewhat small magnitude, current and future technology nodes of semiconductor manufacturing require nanoscale precision and alignment. For example, semiconductor device manufacturing at 22 nm transistor half-pitch has been reported [20]. Even a fraction of a degree temperature rise in the substrate is expected to overwhelm this alignment requirement.

Stress analysis is carried out in ANSYS CFX to determine the thermomechanical stress generated in the wafer due to temperature gradients and thermal expansion mismatch due to the UV heating. Material properties used for these simulations are listed in Table 1. Figure 5 plots the maximum stress as a function of power density. Similar to the variation of peak temperature, it is found that the maximum stress increases with increasing power density, indicating that a low power density dosage delivered over a longer time is preferable to minimize stress generation in the substrate during nanoimprinting. In general, mechanical stress generation in the wafer during nanoimprinting process is undesirable for semiconductor microelectronics, since mechanical stress is known to adversely affect transistor performance [21,22]. Particularly, mobility of electrons and holes reduces due to mechanical stress, resulting in reduced transconductance in MOSFET transistors [22]. Moreover, excessive stress in the wafer can lead to cracking and other catastrophic failure [23].

Note that while the thermal analysis presented above suggests developing a field for longer time at lower power, doing so is in

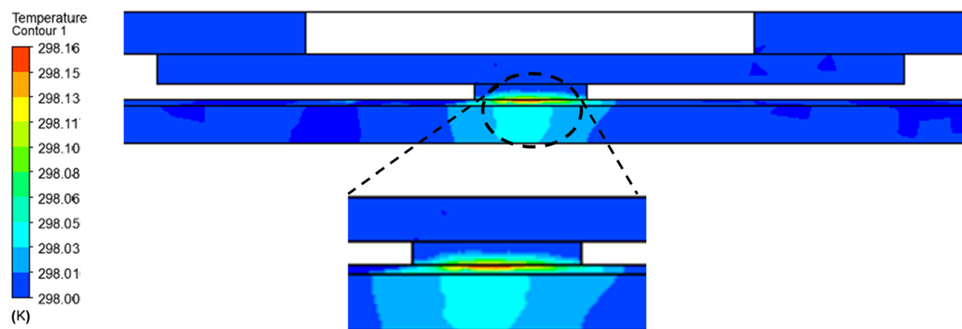

Fig. 3 Cross-section temperature plot of the nanoimprinting geometry indicating the temperature distribution due to the nanoimprint lithography process

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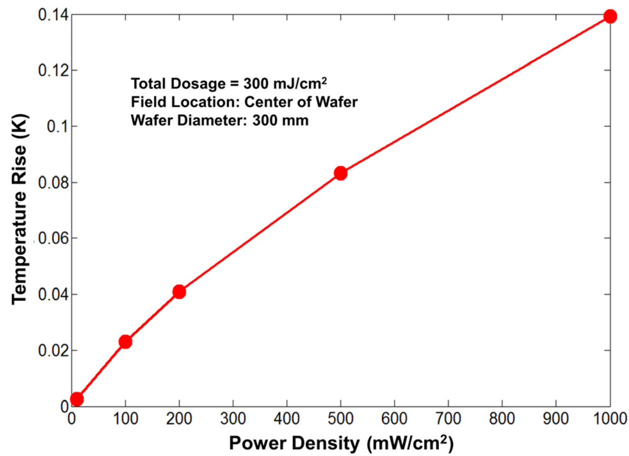

Fig. 4 Plot of the maximum temperature for a number of power density values, for the same total energy density being transferred to the monomer

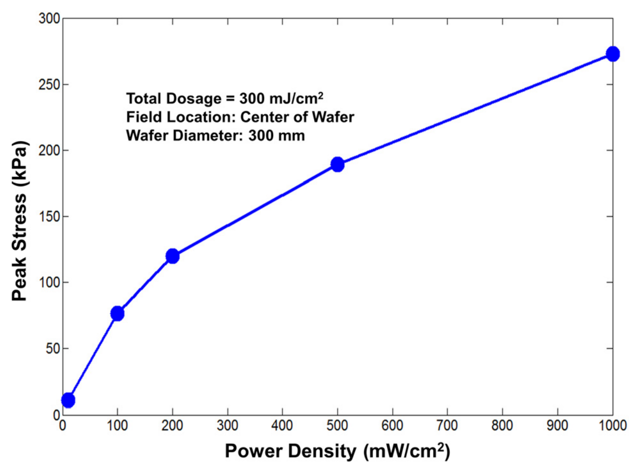

Fig. 5 Plot showing the dependence of maximum stress on power density for the same total energy density being transferred to the monomer

conflict with the system-level requirement of high wafer processing throughput rate. Excess time for exposure allocated in each field adds up over the entire wafer, particularly in 300 mm and 450 mm wafers that have hundreds of fields on each wafer. This restricts the number of wafers that can be processed per hour. However, if the UV exposure time is small compared to other processes such as template motion to the imprint site, etc., then increasing exposure time and lowering exposure power may not significantly reduce throughput since the exposure time is not a rate-limiting step in the overall process. Thus, system-level manufacturing design requires careful consideration and optimization of both thermal performance and throughput.

3 Multifield Exposures and Design Trade-Offs

While the modeling of a single-field exposure provides an understanding of the thermal characteristics of nanoimprinting, further refinement in the model is required for fully capturing the nanoimprint process. Nanoimprinting is inherently a multi-exposure process where several fields are exposed on a single wafer. Each field is size-limited due to restrictions on template size, due to which each substrate may have hundreds of fields that must be exposed in a sequential fashion. A complete understanding of the thermal characteristics of this process requires modeling of multiple sequential field exposures.

While modeling hundreds of field exposures in sequence in a simulation model is computationally intensive, modeling a few samples may be sufficient for providing an understanding of the underlying thermal characteristics of the system. Such an approach also helps identify system-level design trade-offs.

A multifield exposure simulation model for transient heat transfer is developed. In this model, nine adjacent fields of size 10 mm by 10 mm each in a 3×3 matrix are sequentially exposed with a constant power density of 1000 mW/cm^2 for 0.3 s. Figure 6 shows the resulting transient temperature plot. Maximum temperature in each field are plotted in Fig. 6. As expected, Fig. 6 shows that exposure of one field influences at most the immediately neighboring fields, but not other fields. This is along expected lines, since the thermal penetration depth for the exposure time used here is around a few mm. The thermal influence of the field being exposed decays with time. However, if the immediately adjacent field is exposed next, the peak temperature rise of the adjacent field is higher than the previous one, since the previous exposure caused the adjacent field to be already hot when it is exposed.

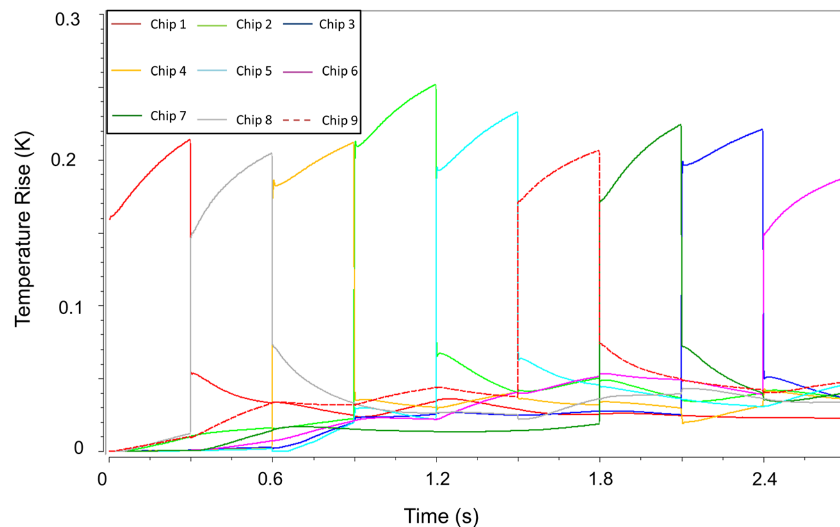

Fig. 6 Transient temperature plot resulting from sequential exposure of multiple fields on a substrate

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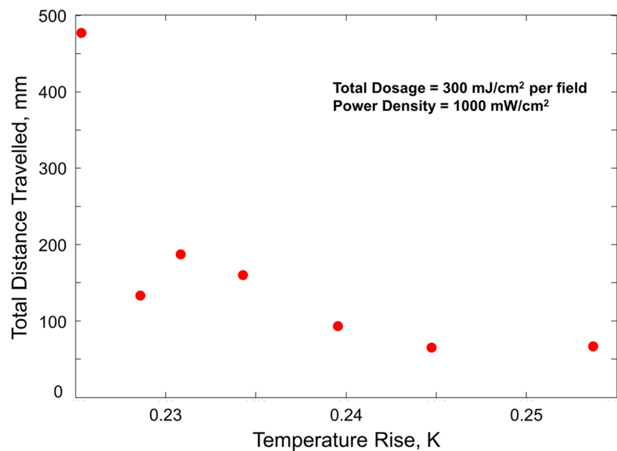

Fig. 7 Plot of peak temperature rise and total distance traveled for seven different sequencing schemes for a seven-field exposure, indicating a fundamental trade-off between thermal design and system throughput

Results shown in Fig. 6 indicate that a sequential strategy for field exposure may not be thermally optimal since it leads to additional temperature rise in sequential fields. Instead, it might be beneficial to choose the farthest possible field at the end of each exposure step for the next exposure. The inherent trade-off in this decision-making process for sequencing is that if subsequent fields being exposed are farther apart, the template travel time will be higher, resulting in reduced throughput. On the other hand, if subsequent fields being exposed are closer to each other, it results in increased throughput, but also higher temperature rise. Figure 7 illustrates this trade-off by plotting the peak temperature rise and total travel time for seven different sequencing schemes for the same nine-field exposure. Schemes include one in which the nearest neighbor is exposed next, and one in which the farthest one is exposed next. Results indicate the presence of an interesting trade-off in one of the schemes where the travel time and peak temperature rise are both fairly low, but not the lowest possible. Figure 7 shows that a heavy penalty must be paid in terms of one of the parameters, if the other parameter is driven to optimality. For example, in going from the second-from-right data point to the right-most data point, there is very little incremental improvement in distance traveled but a very steep penalty in terms of the resulting increase in temperature rise. Similarly, on the left side of the plot, there is marginal improvement in temperature rise going from the second-from-left data point to the left-most data point, but a substantial increase in distance travelled. Thus, a suboptimal solution, where both parameters are close enough to being optimal without actually being optimal may be the most appropriate trade-off between thermal and throughput concerns. A system-level trade-off analysis between temperature rise and throughput will need to take into account other processes occurring during the nanoimprint process, including motion of template and other tools to and from the nanoimprinting site and whether these processes occur sequentially or in parallel with the nanoimprinting process.

4 Conclusion

Nanoimprinting is a promising technology for enabling nanomanufacturing for a variety of engineering applications. The UV exposure process, which is fundamental to nanoimprinting offers significant thermal management challenges that must be addressed in order to obtain overlay accuracy of tens of nanometers or less. In this paper, this problem is analyzed, both at the single field level, and at the multi-field level. Results indicate an inherent trade-off between thermal management and overall throughput. Results presented in this paper are expected to help in developing a firm understanding of thermal management in nanoimprint lithography, which may lead to technological solutions for addressing such trade-offs. Experimental validation of the model presented here is suggested as a possible future work. Such a validation will require measurement of temperature rise as a function of UV power. The temperature measurement scheme should be designed such that it does not alter the temperature field itself. It is expected that this will further help in the development of useful process design rules based on this work.

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