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Effect of Through-Silicon-Via Joule Heating on Device Performance for Low-Powered Mobile Applications

Three-dimensional (3D) through-silicon-via (TSV) technology is emerging as a powerful technology to reduce package footprint, decrease interconnection power, higher frequencies, and provide efficient integration of heterogeneous devices. TSVs provide high speed signal propagation due to reduced interconnect lengths as compared to wire-bonding. The current flowing through the TSVs results in localized heat generation (joule heating), which could be detrimental to the device performance. The effect of joule heating on performance measured by transconductance, electron mobility (e^- mobility), and channel thermal noise is presented. Results indicate that joule heating has a significant effect on the junction temperature and subsequently results in 10–15% performance hit. [DOI: 10.1115/1.4028076]

Keywords: joule heating, TSVs, e^- mobility, transconductance

1 Introduction

Convergence and miniaturization of consumer electronic products such as cameras, phones, etc., has been driven by enhanced performance and reduced microelectronics size. For past few decades, Moore's law has been driving the micro-electronics industry to achieve high performance with small form-factors at a reasonable cost [1]. While the continued miniaturization of the transistors has resulted in unparalleled growth of the electronics industry, further performance increment via size scaling could be cost-ineffective and difficult to manufacture. To satisfy the current/future integrated circuit (IC) package requirements, vertical integration of chips holds the key, i.e., 3D packaging. Chip-stacking (3D) is emerging as a powerful technology to reduce package footprint, decrease interconnection power, higher frequencies, and provide efficient integration of heterogeneous devices. It allows further reduction in the form factor of current systems and eases the interconnect performance limitation since the components are integrated on top of each other instead of side-by-side, resulting in shorter interconnect lengths. To provide shorter/faster interchip thermal–electrical interconnection, TSV technology is being implemented in 3D ICs. Figure 1 shows ITRI's 3D IC roadmap [2]. Heterogeneous integration of devices (memory on logic) looks to be the trend with 3D ICs.

Zheng et al. [3] introduced the development trends of 3D stacked packages. The advantage of 3D over the traditional 2D or planar packaging (multichip-module) and challenges faced by the 3D technology have been discussed. Consumer electronic products such as digital cameras, personal digital assistants, cellphones, etc., require high functional integration in small footprints with low cost. Multichip packaging (chips packaged on the same plane) is one of the solutions. But, due to miniaturization, coupled with the requirements of high memory density, performance, and more features per cm^2 of printed circuit board (PCB), engineers have been forced to think vertically. Stacking dies and interconnecting them vertically accomplishes all of these goals. In 3D technology, chips are stacked vertically in the Z-direction providing a volumetric packaging solution. Due to its reduced size, reduced device cost resulting from increased yield opting system-on-chip (SOC) devices into several smaller area chips, higher electrical performance, and more design freedom for fabricating novel form factors, 3D is gaining popularity in the electronics industry. Alam et al. [4] analyzed the parasitic characteristics of

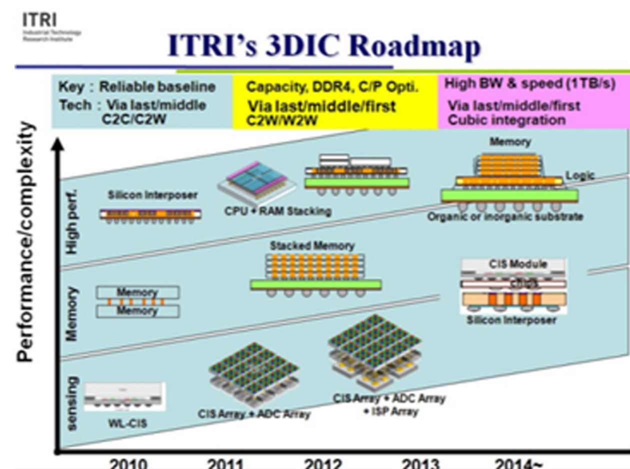

Fig. 1 ITRI 3D IC roadmap [2]

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Contributed by the Electronic and Photonic Packaging Division of ASME for publication in the JOURNAL OF ELECTRONIC PACKAGING. Manuscript received October 22, 2013; final manuscript received July 17, 2014; published online September 19, 2014. Assoc. Editor: Ashish Gupta.

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interdie bonding techniques and materials. Comparing 3D technology with chip scale package, which has a silicon efficiency of about 80%, 3D ICs silicon efficiency is greater than 100% without increasing the thickness or the footprint of the package. Integration in the z direction is achieved by stacking dies or stacking packages and interconnecting them with wire bonding, flip chip, or TSV [3]. For a conventional single chip package, heat can be dissipated through the top (spreader and eventually through the heat sink), bottom (through the substrate and eventually PCB). But for a 3D package used in mobile products, heat dissipation is even more difficult, as heat sink implementation is difficult due to space constraints. TSVs provide better electrical and heat flow path, and are more space and energy efficient as compared to wire bond 3D stacks. The 3D TSV technology reduces the interconnect length and thereby substantially lower the signal delay. Figure 2 shows the technology advantages from planar to the 3D ICs.

Another important aspect of 3D and TSV technology is the cost factor: bonding and via filling has been identified as the costly processes in this technology [5]. Sung et al. [6] studied the thermal distribution in a 3D TSV package with various die stacking architectures. They also analyzed the effect of location and number of TSVs on the maximum temperature of the die. Maximum temperature decreased with TSVs but it was independent of via location. Nagendrappa et al. [7] demonstrated the thermal performance of a 3D package by parameterizing die size, number of TSVs, and solder I/O density. It was demonstrated that the decrease in thermal resistance was small with increase in TSVs alone, but significant improvement was seen when both the TSVs and solder interconnects were increased.

A lot of work is being done in the area of cooling of 3D chip stacks. Matsumoto et al. [8] discussed and evaluated various possible cooling methods from the bottom and periphery of the silicon interposer. Kota et al. [9] presented a parametric study focusing on the design and thermal properties of a liquid interface thermal management solution for 3D stacks using a radial heat sink cooled by an array of synthetic jet actuators. Phan and Agonafer [10,11] developed a novel cooling method for 3D ICs using a multidimensional thermoelectric cooler. Brunschwiler [12] have developed a water cooling technique for effective thermal management of 3D chips, which can enhance the system performance beyond the predicted limits by piping water between each of the 3D layers.

As stated earlier, device performance is a function of several parameters and varies with the junction temperature and the performances decreases with increase in temperature. Karajgikar et al. [13] showed correlation between the temperature and performance for a 90 nm technology Pentium IV Northwood architecture.

Electron mobility (e^- mobility) variation with doping concentration and temperature is shown in Figs. 3 and 4, respectively [14]. Electron mobility is a measure of how fast the electrons would move when excited by a voltage drop, i.e., e^- drift velocity. Thermal variation causes the change in metal resistivity leading to a change in the DC drop [4]. Figure 5 demonstrates the metal resistivity variation with temperature. Mirza et al. [15] demonstrated the effect of junction temperature and TSV diameter on the interconnect delay.

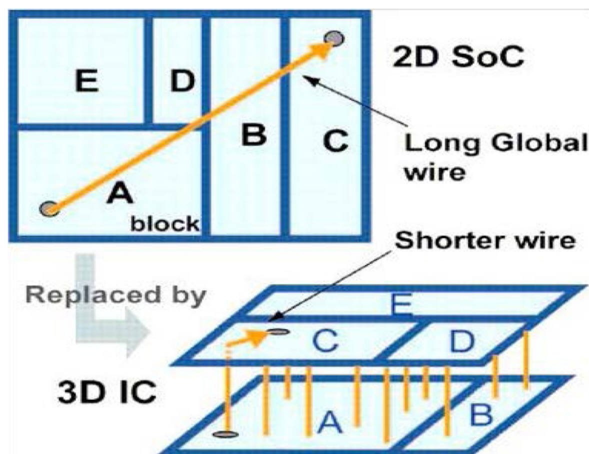

Fig. 2 Comparison between 2D and 3D packages [16]

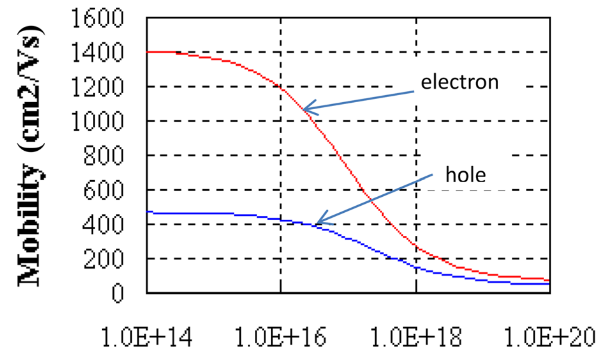

Fig. 3 Variation of e^- and hole mobility with doping concentration (cm^{-3}) [14]

There is a need to determine if TSV Joule heating (caused when current flows through it) is significant enough to cause a substantial change in the junction temperature and eventually leads to performance degradation. In this paper, the effect of TSV joule heating (Eq. (1)) on the device performance parameters: transconductance, e^- mobility, and thermal noise is analyzed. TSVs occupy approximately 1.5% of the chip real estate (CRE) and the TSV diameter is 10 μm with 1 μm thick dielectric around it. In this paper, we limited the TSV area to <4% so we do not inadvertently affect the silicon efficiency.

2 Thermal Modeling

Thermal distribution in the package is analyzed for different TSV currents including a baseline case of no-current through the TSVs and the junction temperature is determined for each case. Due to the difficulty of resolving the length scales, the thermal modeling is performed in two steps using multilevel finite element modeling:

(1) *Global model*: The quarter symmetry 3D model with a 46×46 TSV array is solved for the temperature distribution.
(2) *Submodel*: A subregion in the global model is cut, results from the global model are transferred as boundary conditions to the submodel cut faces, and the submodel is resolved to achieve the final response.

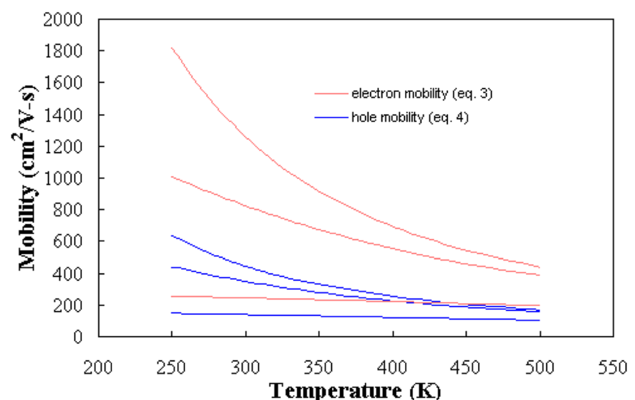

Fig. 4 Variation of e^- and hole mobility with temperature at different doping concentrations (top curve: 10^{16}, 10^{17}; bottom: 10^{18} cm^{-3}) [14]

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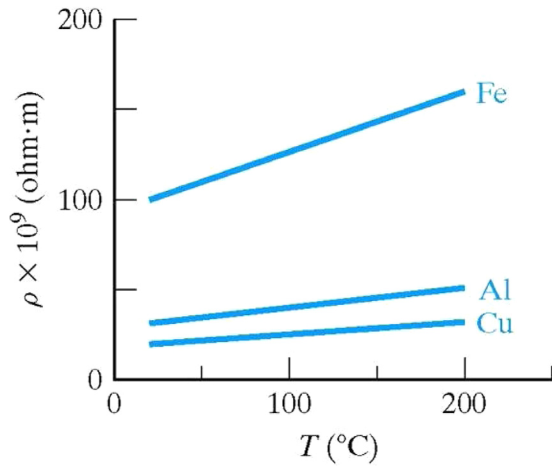

Fig. 5 Variation of resistivity with temperature [20]

The response from the thermal analysis is correlated to the device performance using the correlations available in the literature (discussed in Sec. 3). An understanding of the chip performance dependence on TSV joule heating is developed through this work. This work would lead to an upstream guideline for the front-end-of-line layout

$$\text{Joule Heating}: Q(\text{Joule}) = I^2 R \tag{1}$$

where I is the current through TSV (A) and R is the TSV resistance (ohm).

The thermal analysis was done with the commercially available code ANSYS WORKBENCH v14.5. The test vehicle consisting of substrate, two stacked dies, TSVs, underfill/pillar effective block (Cu and Pb-free solder cap), and the mold was formulated. Each die had an area of 49 mm^2 with 100 μm thickness. TSV diameter was 10 μm with 1 μm thick oxide insulation and a pitch of 75 μm [2]. Substrate and the interdie bond layers (interconnects) were modeled as effective blocks with calculated values of effective thermal conductivity [15]. This was done to achieve the desired accuracy within a reasonable computational time. A quarter symmetry global model was formulated, as shown in Fig. 6.

Figure 7 shows the cross-sectional view of the model. Figures 8 and 9 show the meshed model and TSV. Quarter symmetry model had about 2000 TSVs with mesh count of 125,000 elements. Adiabatic boundary condition was applied at the symmetry faces, and each die was thermally loaded with uniform power, so as to have power of 1 W in the top die (2 W/cm^2) and 3 W, 2 W, and 1 W in the bottom die (6 W/cm^2, 4 W/cm^2, and 2 W/cm^2, respectively). TSV joule heating has been modeled as internal heat generation. Thermal analysis was performed as a natural convection problem with a convective heat transfer coefficient value of 8 W/m^2 K at the exposed surfaces of the overmold. PCB has not been modeled in the analysis. To compensate for the PCB area, a higher "h" value has been used for the substrate bottom/side faces. Ambient is at 22 °C. Material properties for the package components were derived from the literature and are given in Table 1 [15–18]. Submodel is cut from the global and remodeled in detail to include the dielectric insulation around the TSV, metal interconnects between the top and bottom die and between the substrate and bottom die. Schematic of the submodel is shown in Fig. 10.

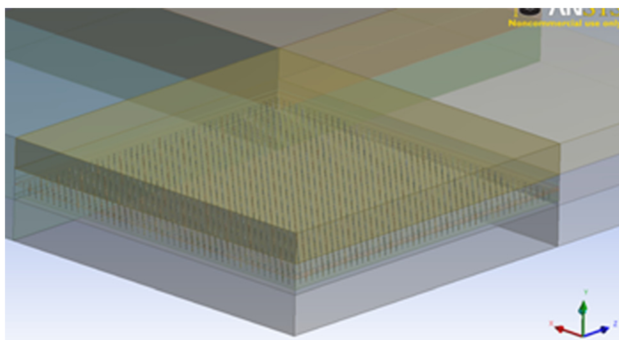

Fig. 6 Quarter symmetry model showing symmetry faces

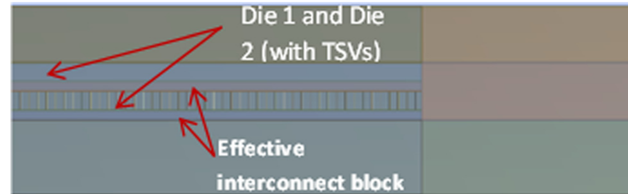

Fig. 7 Model cross section

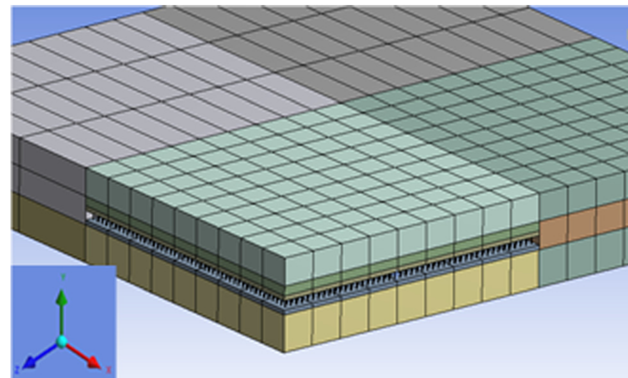

Fig. 8 Meshed model (global)

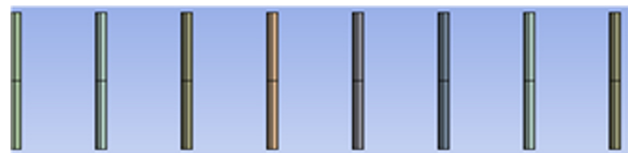

Fig. 9 Meshed TSV (global)

Table 2 shows the various cases that are analyzed in this study. In all the cases, the TSVs were laid out in an area array configuration with uniform pitch. Mesh sensitivity analysis was done for the base case (no TSV current) and an optimal mesh count of 125,000 elements was used for all the design points. The results from the optimal meshed model were transferred as boundary conditions to the submodel and the submodel computed to achieve a more accurate thermal response.

Table 1 Material properties

Material	Thermal conductivity (W/m K)
Substrate	44 (in plane) 3 (out-of-plane)
Underfill	3
Die	130
Mold cap	1
SiO_2	1.3
TSV—Cu	398
Solder (SAC 405)	57

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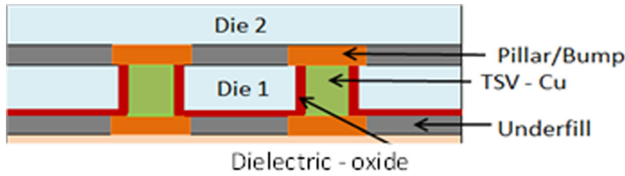

Fig. 10 Submodel—2 × 2 TSVs (detailed geometry)

3 Device Performance

Device performance is a measure of the signal processing speed of the device. Performance parameters include e$^-$ mobility, drift velocity, transconductance, signal delay (interconnect delay), and channel thermal noise. The device performance is affected by interconnect and transistor delay. Transistor delay is a function of transistor gate length and temperature. Interconnect delay varies with the interconnect material, interconnect size, and temperature. Mirza et al. [15] showed the effect of junction temperature and TSV diameter on the interconnect delay through the TSV. Transconductance is the ability of a transistor to deliver amplification or gain, the higher the better. It also determines the rate of switching of the transistor. e$^-$ mobility and drift velocity determines the speed of the electron flow when a voltage drop is induced across it. With excess heat, resistance of the TSV interconnects increases causing increase in the joule heating, which is proportional to the resistance and the square of the current. Thermal noise is caused due to parasitic gate, drain, and source resistance. The dependence of the performance parameters on the temperature is shown in Eqs. (2)–(4) [19,20]. In all cases, the performance parameter variation with the temperature results in performance decline.

$$\mu(T) = \mu(T_0) \cdot (T/T_0)^{-1.5} \tag{2}$$

$$\beta(T) = \beta(T_0) \cdot (T/T_0)^{-1.5} \tag{3}$$

$$\sqrt{\nu^2} = \sqrt{8.k.T}/\left\{\sqrt{(3 \cdot \sqrt{(2 \cdot \beta \cdot I)})}\right\} \tag{4}$$

where $\mu(T)$ is the e$^-$ mobility parameter, $\beta(T)$ is the transconductance parameter, ν^2 is the channel noise, T is the transistor operation temperature (K), I is the drain current (A), k is the Boltzmann constant, and T_0 is the transistor operation temperature—base case (K).

4 Results

4.1 Global Model Results. A 3D quarter symmetry model of the 3D IC with approximately 8000 TSVs is formulated in Ansys. Different configurations (with varying TSV current) and the baseline case with no TSV current (TSVs considered as the thermal path only) are simulated and the thermal analysis is performed to estimate the junction temperature. Temperature distribution in the package is analyzed to demonstrate the heat flow path. The overall area occupied by the TSVs is 1.5% of the chip area. The uniform chip power is 1 W for the top die and 3 W, 2 W, and 1 W for the bottom die (die with TSVs). Heat transfer coefficient value is used at the exposed surfaces to model the convective heat transfer to the environment. The aim of this study is to determine if TSV joule heating could significantly affect the maximum die temperature, and if so, by how much. Mesh sensitivity analysis was performed, and an optimal mesh of 125,000 elements was used for all the cases.

Table 2 Design of experiments (TSV pitch = 75 μm)

Case	Top die power (W)	Bottom die power (W)	TSV diameter (μm)	TSV current (mA)			
1	1	3	10	0	20	40	60
2	1	2	10	0	20	40	60
3	1	1	10	0	20	40	60

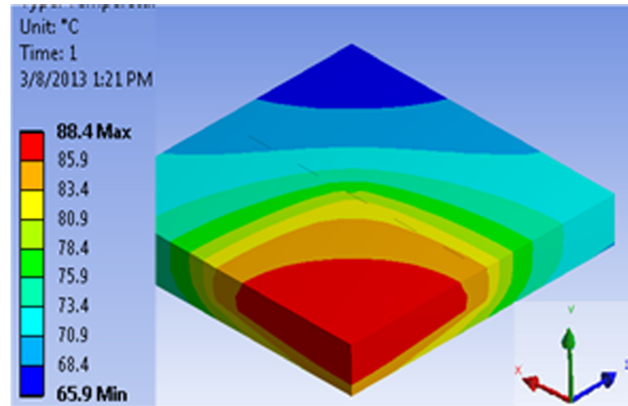

Fig. 11 Temperature distribution—package (no TSV current)

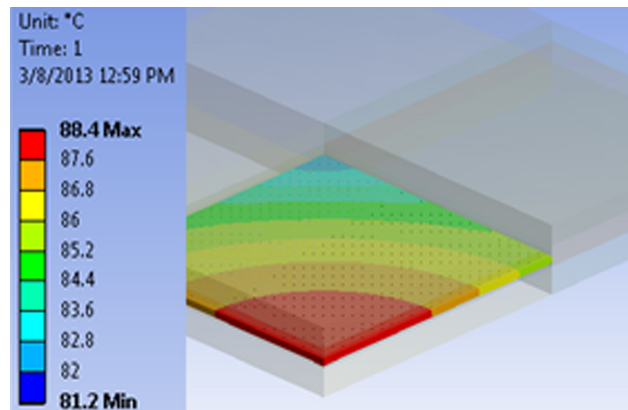

Fig. 12 Temperature distribution—bottom die (no TSV current)

Figures 11 and 12 show the temperature distribution in the package and the bottom die for the baseline case (no TSV current) for a chip power of 4 W. Junction temperature in the bottom die is found to be 88.4 °C for the baseline case while 99.3 °C for the 40 mA TSV current case. Figures 13 and 14 show the temperature distribution for the 40 mA case.

Full field thermal analysis results show a 11 °C increment (12% increase) in the junction temperature between the baseline and the 40 mA case when the total package power is 4 W. Figure 15 demonstrates the junction temperature (max temperature in the die)

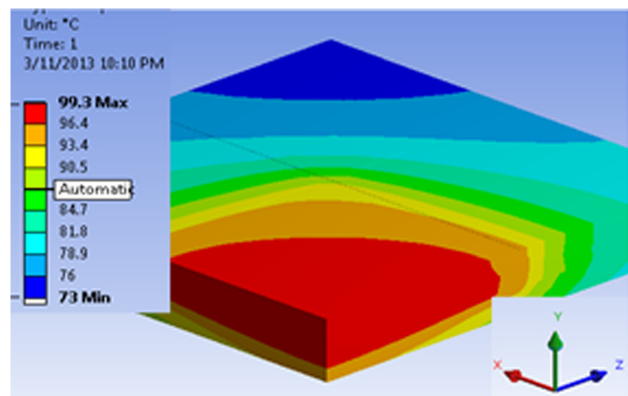

Fig. 13 Temperature distribution—bottom die (40 mA TSV current)

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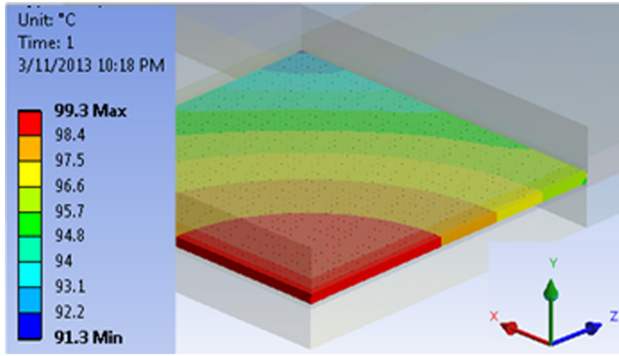

Fig. 14 Temperature distribution—bottom die with TSVs (40 mA TSV current)

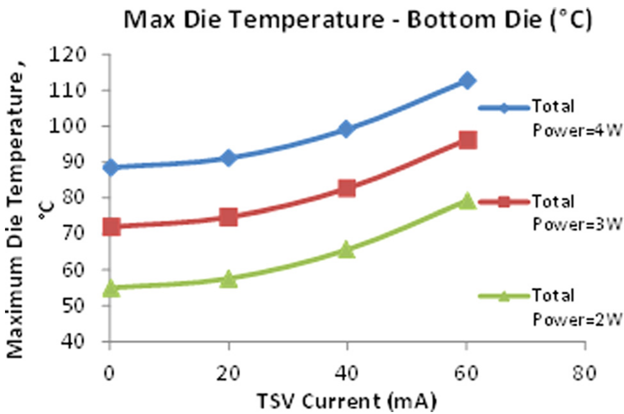

Fig. 15 Maximum temperature for various chip power—global model

variation with the TSV current for all the cases analyzed (i.e., total power = 2 W, 3 W, and 4 W). As expected, the temperature increases with higher TSV currents, and the difference was significant. Approximately 24 °C difference is seen between the baseline and the 60 mA design point for all the cases. A difference of ~8 °C is seen between the TSVs at the center and the periphery. From Fig. 15, it is evident that the variation in the junction temperature with TSV current is independent of the total power of the package. Figure 20 shows that the performance hit from the baseline case (no TSV joule heating) is constant with the chip power.

4.2 Submodel Results. A section of the global 3D model was submodeled—2 × 2 TSV array as shown in Fig. 16 with detailed TSV, dielectric layer, and Cu-pillar interconnect features. These features were not present in the global model due to scale difference between various components of the package. Submodel

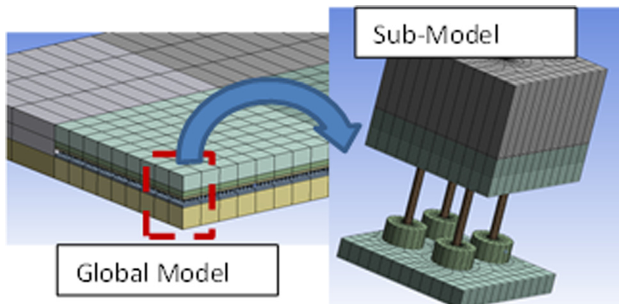

Fig. 16 Meshed global and submodel

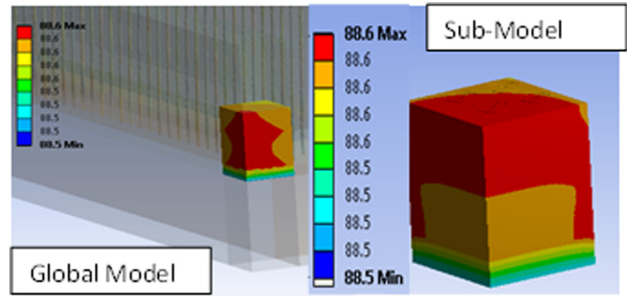

Fig. 17 Temperature distribution—comparison between global and submodel response (no TSV current)

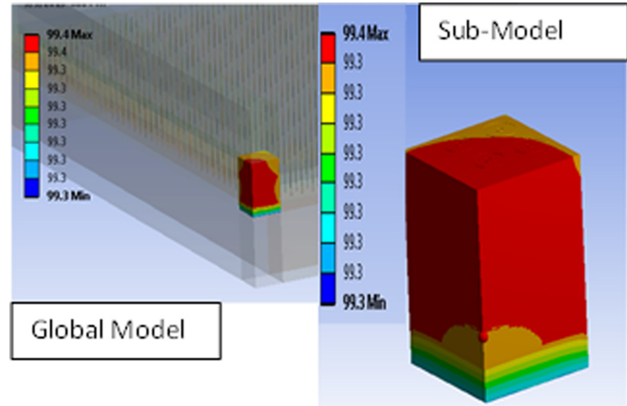

Fig. 18 Temperature distribution—comparison between global and submodel response (40 mA TSV current)

consist of the two chips, Cu-pillar interconnects, detailed TSV feature, and the oxide insulation. Submodel results in Figs. 17 and 18 clearly indicate that there is negligible difference in the junction temperature between global and the submodel. It shows that the effective properties (thermal conductivity values) used for the TSVs and Cu-pillar interconnect was reasonably accurate and also the finer meshing in the submodel did not affect the thermal response.

Using Eqs. (2)–(4), the junction temperature increase with joule heating is correlated with device performance. Figure 19

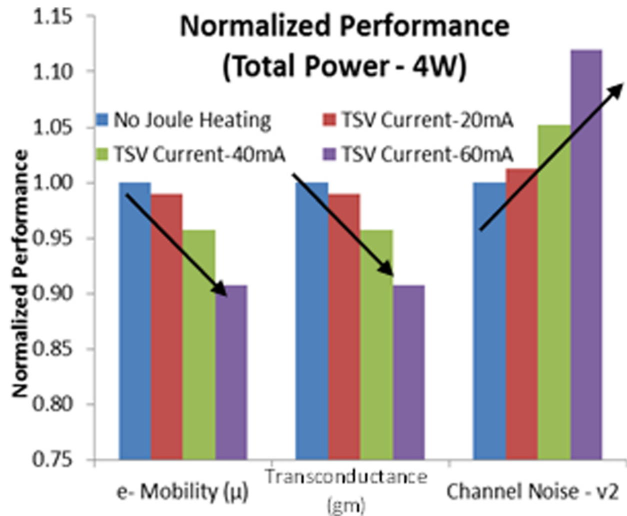

Fig. 19 Variation in performance with TSV joule heating for 4 W total power

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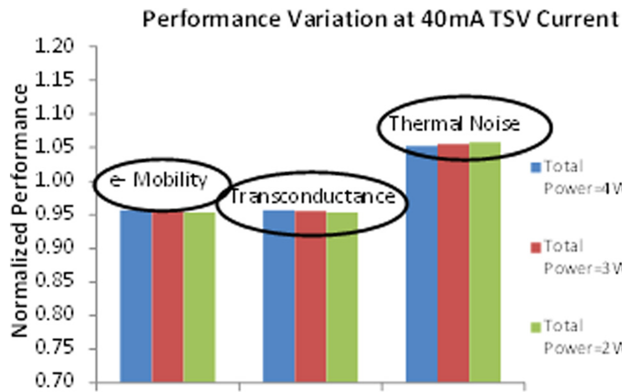

Fig. 20 Variation in performance hit with chip power for 40 mA case (normalized to the baseline case)

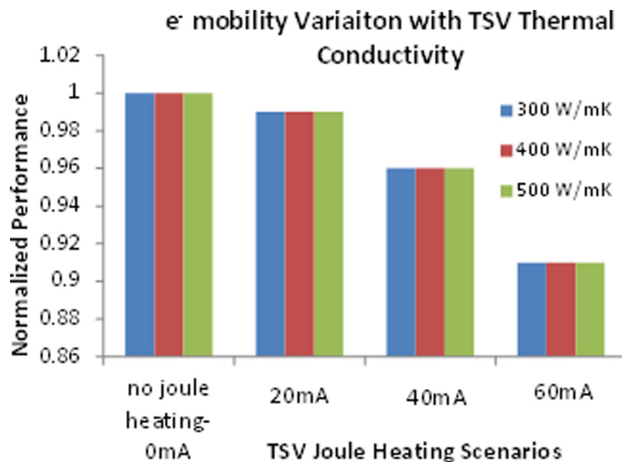

Fig. 21 Variation of e$^-$ mobility with TSV thermal conductivity

demonstrates the variation of the performance parameters: e$^-$ mobility, transconductance, and channel noise with the TSV current (0–60 mA). Almost 10% performance hit is observed for e$^-$ mobility and transconductance and ~15% for the channel thermal noise between the baseline and the 60 mA case. Figure 20 shows that the performance hit variation (at constant TSV current) showing joule heating effect is independent of chip power. Furthermore, the effect of the TSV thermal conductivity on the thermal and device performance of the 3D TSV IC was also studied.

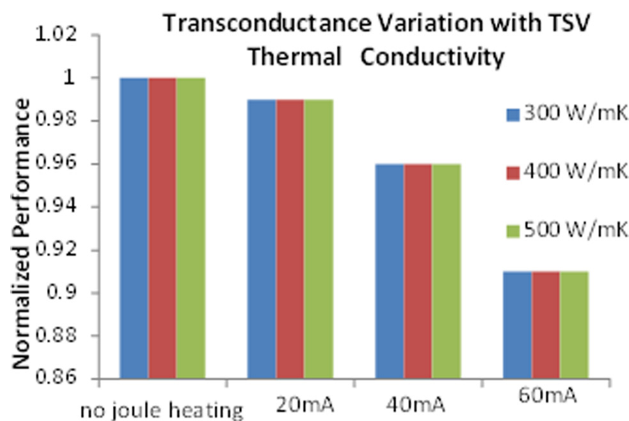

Fig. 22 Variation of device transconductance with TSV thermal conductivity (at different joule heating scenarios)

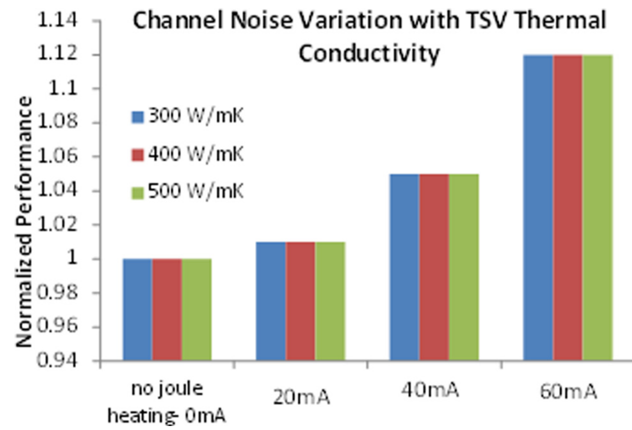

Fig. 23 Variation of channel noise with TSV thermal conductivity (at different joule heating conditions)

Since TSVs occupy 1.5% of the CRE, the majority of the heat is conducted through the silicon (~98.5% of the chip area). Therefore, variation of the TSV thermal conductivity does not have any significant effect on the overall temperature profile of the package. The junction temperature shows negligible change when the TSV thermal conductivity is varied, thereby having no effect on the device performance. Figures 21–23 show that the e$^-$ mobility, transconductance, and the channel noise is independent of the TSV thermal conductivity. This tells us that TSVs are primarily the signal carriers and the majority of the heat dissipated is through the silicon owing to the TSVs small area.

5 Conclusion

There is a significant move to introducing 3D stacking in a variety of electronic systems. Most of the products in the market are low power devices and utilize wire-bond for interconnects. As we start migrating this technology to more general systems, the use of TSVs is critical in both increasing the number of interconnects per area (peripheral versus area) as well as improving the thermal/electrical performance. In this paper, thermal–electrical analysis of a 3D IC with TSVs is demonstrated. It is clearly evident that joule heating has a significant contribution to the overall heat in the package, thereby causing a significant die temperature increase. Joule heating can cause a temperature increase of up to 25 °C when compared with baseline (no TSV current case). Correlation of temperature variation with the chip performance has been performed, and three performance parameters have been analyzed. A 10–15% performance hit is seen between the baseline and the 60 mA case for various performance parameters. The performance hit variation (at constant TSV current) is negligible with the chip power, i.e., performance hit due to joule heating is independent of chip power, and that it only depends on the TSV resistance and current. The temperature and the device performance degradation are practically independent of the TSV thermal conductivity owing to the fact that TSVs occupy a very small area on the die, and that the majority heat dissipation is through the silicon. Interestingly, there is negligible difference between the global and the submodel thermal response, thereby suggesting that the global level thermal analysis is sufficient for such systems.

Acknowledgment

This material is based upon work supported by the National Science Foundation under Grant No. CBET-1236370.

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