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# Experimental investigation of electromigration failure in Cu–Sn–Cu micropads in 3D integrated circuits

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## ABSTRACT

Inter-die electrical communication in vertically-stacked three-dimensional integrated circuits (3D ICs) is facilitated by inter-die micro bumps. The electromigration reliability of micro bumps is critical for developing an understanding of reliability of 3D IC based microelectronic systems. This paper reports experimental investigation of electromigration reliability of Cu–Sn–Cu microbumps formed between two die by thermo-compression bonding. The two-die 3D IC is assembled in wire bond ceramic packages and electromigration tests are conducted in both air and nitrogen ambient at various temperatures. Failure lifetime and Mean Time To Failure (MTTF) of microconnect chains and Kelvin structures are measured. Results indicate that the intrinsic activation energy of Cu–Sn microconnects is between 0.87 eV and 1.02 eV. Based on failure analysis, possible failure mechanisms are proposed. Results presented in this work are expected to improve the fundamental understanding of electromigration reliability in 3D ICs and facilitate the development of robust and reliable microelectronic systems based on 3D ICs.

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# 1. Introduction

Vertically-integrated three-dimensional microelectronic systems have attracted a significant amount of research in the recent past. This technology is enabled by bonding of multiple strata to one another, and by connecting circuits on each die using interdie bond pads and through-stratum vias (TSVs). The inter-die bond is a critical part of this process technology, as it enables rapid electrical interconnection besides providing mechanical integrity of the inter-die bond. Much of the 3D IC process research in the past 1–2 decades has focused on developing rapid, high-yield manufacturing processes for inter-die bonds and TSVs [1–4]. More recently, electrical design methodologies for 3D IC based systems have also been developed [5,6].

Implementation of 3D IC technology in next-generation products requires a thorough understanding of reliability performance of inter-die bond layers. This includes a fundamental understanding of the mechanisms behind bond failure as well as a systematic experimental investigation of failure rates of inter-die bonds. Such an approach helps establish the current carrying capacity of the inter-die microbumps, and helps determine life time and failure rates.

Electromigration is a primary driving mechanism affecting the reliability of traditional die and package interconnects such as last-metal Cu interconnects and die-to-package C4 bumps [7,8]. Electromigration occurs when conducting atoms move as a result of momentum transfer from current carrying electrons. The intrinsic electromigration reliability of last-metal Cu interconnects is mainly limited by Cu diffusion at the Cu/nitride interface while dominant reliability issues for die-package solder bumps are current crowding and Joule heating at the under bump metallization (UBM) [8]. Electromigration may also play a significant role in determining the reliability of 3D interconnection technology based on micro-bumps, which are larger in size than last metal Cu interconnects but not as large as Pb-free Sn-Cu solder bumps that provide die-to-package interconnection. Due to the unique length scale of inter-die micro-bumps, it is important to study their electromigration behavior since models for neither last metal interconnects nor die-package solder bumps may apply.

Accelerated electromigration testing is usually carried out under the assumption that failure modes in accelerated failures and regular failures remain the same. A summary of various reliability related challenges in 3D IC technology has been reported [9]. Chao *et al.* have presented a review of recent work on electromigration related reliability in microelectronic devices [10]. Vertical interconnection through micro-bumps is identified as a major enabling technology for which reliability is not well studied. It is known that







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intermetallic formation is a major cause of bond failure [10]. However, only a limited amount of experimental work in this direction is available. Thermal cycling reliability of microbumps has been reported in the recent past [2,3]. Electromigration studies on inter-die bonds in 3D ICs have been reported [11–14]. The effect of intermetallic formation on electromigration reliability of the inter-die bond layer in 3D ICs has been investigated [15–17]. Material and structure dependence of reliability performance of microbumps in 3D IC technology has been reported [13]. Electromigration in Ni–Sn [18] and Sn–Ag [19] based microbumps has been studied.

This paper presents experimental results on electromigrationdriven reliability of Cu-Sn-Cu microbumps in a two-die 3D IC. The Cu–Sn–Cu micro-connects are formed by thermal compressive bonding [20]. Microconnect chains and Kelvin structures are used for electromigration testing. Failure mechanisms are identified and compared with well-known failure mechanisms in last metal Cu-interconnect and solder-bumps. The intrinsic activation energy of Cu-Sn microconnects is measured to be in the range of 0.87-1.02 eV. The microbumps studied in this work fail primarily due to voiding caused by Cu through the TiW diffusion barrier. It is found that failed Kelvin structures show voiding in both the microconnects and in the associated last metal connections to the microconnects. Section 2 presents a brief description of the two-die 3D IC, test structures and other experimental details. Section 3 discusses results from electromigration testing of the microbump chain structures.

## 2. Experimental setup

An SEM cross-section image of the microconnect used in experiments is shown in Fig. 1(a). The cross-section is generated using a Focused Ion Beam (FIB). Fig. 1(b) shows a schematic of the microconnect bonding process. The stratum on the bottom is referred to the acceptor die, and the one on the top is the donor die. Both dies are fabricated with 90 nm CMOS technology on 200 mm wafers. Following fabrication, the wafers are thinned to 280  $\mu$ m. The acceptor and donor die are then diced into 7.5 × 7.58 mm<sup>2</sup> and 6.54 × 6.54 mm<sup>2</sup> sizes respectively. On the acceptor wafer, 5  $\mu$ m Cu pads are formed over passivation openings of the inlaid Cu traces of the microconnect chain structures. On the donor die, except for the 5  $\mu$ m Cu pads, another 3  $\mu$ m Sn is deposited by electroplating Cu and Sn in photoresist defined openings onto TiW barrier

and Cu seed layers. Probe and wire bonding pads are also formed on the perimeter of the acceptor die and connected to the chains with Cu traces via aluminum capped Cu pads. After thermo-compression bonding, a Cu–Sn intermetallic layer joins the microconnects between the acceptor and donor die to serve as both an electrical and mechanical connection, as shown in Fig. 1(a).

Electromigration experiments are carried out using die-to-die microconnect chains and Kelvin test structures with 15 µm and 25 µm square micropegs in the test chip. Microconnect chain structures, typically composed of at least 1000 microconnects, are primarily used to identify the weakest link in the chains. Microscopic images of the chain structure for 15 µm and 25 µm micropads are shown in Fig. 2(a). Kelvin structures are used to study the intrinsic failure of the microconnects, for which the schematic design is shown in Fig. 2(b). In the current work, two microconnects are placed on the sense side and one on the force probe, forcing electromigration stress mostly on the force side. After assembling the thermal-compressive bonded 3D die pairs into wire bond ceramic packages, electromigration tests are conducted in both air and nitrogen ambient from 175 °C to 350 °C in a commercially available electromigration test system. The current induced Joule heating of the structures is first tested as a function of stress current. The results, shown in Fig. 2(c) follow the expected  $I^2$ dependence, with no significant difference between 15 µm and 25 µm micropads. However at a given current, chain structures display significantly higher Joule heating than Kelvin structures. Above 120 mA, chains deviate from the  $I^2$  curve and quickly break down due to several Joule heating. This provides stress current limits that can be used for electromigration testing. Electromigration testing is carried out with 75 mA current on both 15  $\mu$ m and 25  $\mu$ m micropads, resulting in current densities of  $3.3 \times 10^4$  A/  $cm^2$  and  $1.2 \times 10^4$  A/cm<sup>2</sup>, respectively. The time to failure in the lifetime test is defined as the time when the resistance exceeded 10% of the original resistance. For each test, over 28 samples are measured in identical conditions for statistical analysis.

## 3. Results

#### 3.1. Electromigration testing of microconnect chain structures

The electromigration test for microconnect chain structures provides an indication of the weakest link that fails earlier than

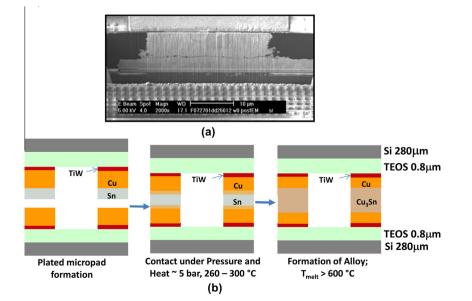


Fig. 1. (a) SEM image of a typical Cu–Sn–Cu microconnect, (b) Cu–Sn–Cu microconnect bonding process and conditions.

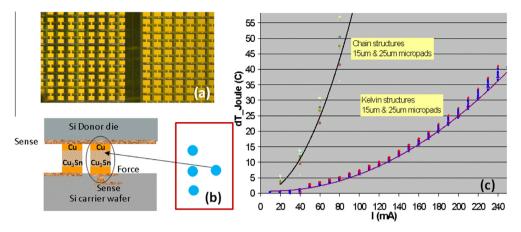


Fig. 2. (a) Microscopic image of the chain structure. (b) Schematic of a Kelvin structure. Three bumps at the sense electrode, and one bump at the force electrode. Force bumps experience the most electromigration stress. (c) Joule heating measurement for the 15 µm and 25 µm microconnect chains and Kelvin structures.

any other link. This is used to determine the early Cu-Sn failure mode in the microconnects. The test is initially conducted in both air and N<sub>2</sub> ambient at 300 °C and 350 °C. Fig. 3(a) shows the change in resistance as a function of time for a chain at 300 °C in both air and N<sub>2</sub> ambient. All curves show a slight increase in resistance over time followed by a sharp increase in resistance. Fig. 3(b) shows a SEM image of one micropad tested for over 100 h at 300 °C air ambient, resulting in metal whisker growth on the side wall. The lifetime Cumulative Distribution Functions (CDFs) are plotted in Fig. 4 for air at 300 °C and 350 °C. CDF for nitrogen ambient at 300 °C is also plotted. These CDFs show longer mean time to failure (MTTF) in N<sub>2</sub> ambient compared to air, thereby indicating that oxidation of Cu-Sn microconnects may be a significant factor in the electromigration failure mode in an air ambient [21-24]. MTTF also reduces at 350 °C in air compared to 300 °C in air, which is attributed to thermal activation due to increased temperature.

Voltage contrast and Electron Diffraction Spectroscopy (EDS) tests are conducted on the post-electromigration samples in order to identify the failure site and failure mechanisms on the micro-connect chain after electromigration testing. The voltage contrast test is a powerful technique to locate failure spots on a large microconnect chain. In the test, electrons are injected from one side of the chain. If a failure spot is encountered, the electrons accumulate on one side of the chain, forming a charging contrast with the other side of the chain, which is electrically disconnected from the electron charges. Fig. 5(a) shows a voltage contrast SEM image of a microconnect chain after electromigration testing in  $N_2$  ambient at 300 °C. One side of the change appears

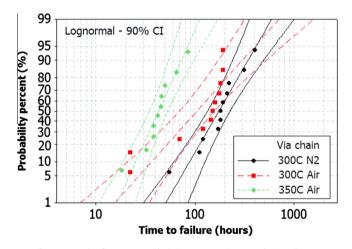


Fig. 4. CDF plot for 25 µm-pad chain structure in N2 and air ambients.

as white streaks in a dark background due to electron charging, and the failure spot can be easily located at the contrast joint. The failure spot is then cut with a focused ion beam (FIB) to inspect its cross-section, shown in Fig. 5(b). Large voids are seen in the  $Cu_xSn_{1-x}$  alloy after electromigration stress, whereas Cu diffuses to the sidewalls of the microconnect during electromigration. EDS of these failure spots reveals that the sample tested in air ambient has a greater oxygen component than the ones tested

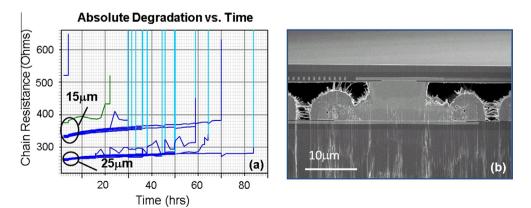


Fig. 3. (a) A typical chain resistance trace versus time during EM stress test. (b)SEM plot of a microconnect after 350 °C of thermal heating for more than 100 h.

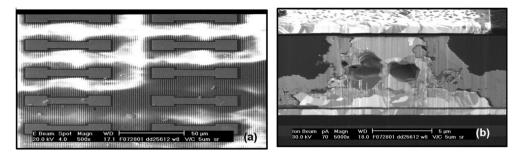


Fig. 5. Voltage contrast test results for a via chain structure. (b) Voltage contrast SEM image of a via chain. The white color occurs due to the charging of electron from one side of the chain.

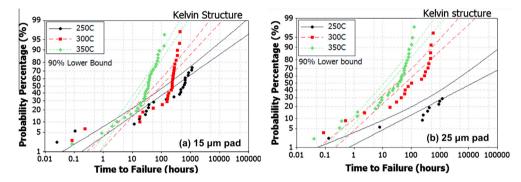


Fig. 6. CDF plot for (a) 15 µm and (b) 25 µm Kelvin structures from electromigration testing at 250 °C, 300 °C, and 350 °C.

in  $N_2$ . As oxygen interaction affects the determination of the intrinsic reliability characteristics, further electromigration testing is conducted only in a  $N_2$  ambient.

#### 3.2. Electromigration testing of Kelvin structures

Kelvin structures are initially designed on the chip to measure single via contact resistance, which can be used to determine the intrinsic failure mechanics in electromigration testing. The structure used in the electromigration test has two connections on the sense probe and one on the force probe. As a result, the force micropad experiences higher current flow, resulting in higher electromigration stress and earlier fails than other vias. Fig. 6(a) and (b) shows the electromigration lifetime CDF plot of the Kelvin structure at 250 °C, 300 °C and 350 °C for 15 µm and 25 µm micropads, respectively. The failure lifetimes show bimodal behavior. Except for a few early fails among a large sample size, most microstructures fail following one activation energy, and very likely the same failure mechanism. It is to be noted that for the 25 µm micropad, the 250 °C electromigration test is terminated after running for 1200 h with less than 50% failed. Based on the mean time to failure (MTTF) using Black equation [7], the intrinsic activation energy of such Cu-Sn microconnects is estimated to be 0.87 ± 0.16 eV for 15  $\mu$ m micropads and 1.02  $\pm$  0.20 eV for 25  $\mu$ m micropads, excluding the early failure data points. The activation energy is comparable to the Cu metallization [25-26] and is higher than a normal Pb-free solder joint at such current density [27]. However, if the early failure modes are included, this activation energy is reduced to 0.5 eV. Lifetime extrapolation based on this data shows that a 1000 ppm fail rate can be achieved after 10 years of life at 105 °C.

After electromigration testing, failure analysis for the Kelvin structures with different lifetimes is carried out by dicing the samples with focused ion beam (FIB). SEM images of microconnect cross-sections are shown in Fig. 7(a)–(c). Fig. 7(a) shows the cross-section of a die without any electromigration testing. An early electromigration failure mode location is shown in Fig. 7(b), and a nominal electromigration failure mode is shown in Fig. 7(c). Electron flow direction is marked on the figure to assist the understanding of the electromigration process.

Before electromigration testing, the Cu-Sn microconnect is intact, and the Cu-Sn intermetallic region is located at the center of the microconnects, sandwiched between the two Cu micro-pegs of the donor (top) and the acceptor (bottom) dies, with only small Kirkendall defects at the bond interface. In the early failure mode, electron flow is applied from the acceptor to the donor die as shown in Fig. 7(b), causing large voids in the Cu last metal layer and between the TiW/Cu-Sn interface near cathode (lower micropad) and leaving the TiW barrier hanging on the dielectric. However the last metal on the anode side (top micropad) is intact. Also, the Cu micropegs from both the acceptor and donor die appeared to migrate to the sidewall of the microconnect, following the electron flow direction. It is likely that the clustering of  $Cu_{x-1}$  $Sn_{1-x}$  intermetallic near the cathode micropad is due to the Cu migration. In the nominal failure mode where most electromigration stressed parts fail, the Cu-Sn intermetallic region expands more uniformly between the donor and acceptor dies, as shown in Fig. 7(c). Besides voids in the last metal layer at cathode, voids are also formed at the last metal and micro-peg near anode, where these regions are originally filled with Cu. With the electromigrating stress, Cu migrates more aggressively to the sidewall of the microconnect, leaving only the  $Cu_xSn_{1-x}$  intermetallic in the middle. The boundary between Cu and  $Cu_x Sn_{1-x}$  intermetallic also becomes more evident, and voids and gaps appear at the boundary interfaces. An EDS plot of nominal failure mode samples after electromigration testing is shown in Fig. 7(d). This plot shows a Cu rich material accumulated at the microconnect sidewalls after electromigration testing.

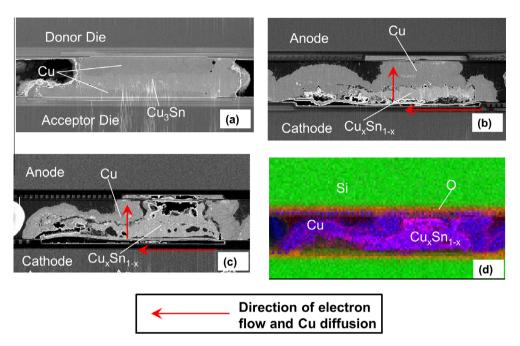


Fig. 7. Failure analysis of Kelvin structures: (a) SEM of a microconnect before EM testing, (b) after EM testing in early failure mode, (c) in nominal failure mode. (d) EDS result for Kelvin structures after EM testing.

## 4. Discussion

Electromigration failures show void formation in the last metal connections as well as within the microconnects. Microconnects in the nominal failure mode are observed to have more cumulative voiding within the microconnects and in the last metal connections on both the acceptor and donor sides of the microconnects. Void formation in the last metal layers suggests movement of Cu through the TiW diffusion barrier under the electromigration stress, however this study does not incorporate different TiW barrier thickness in this study to evaluate Cu diffusion through the TiW barrier. The wide lifetime log-normal distribution of the early failure samples in 3D microconnects suggests that more in-depth understanding of failure modes may assist in improving the electromigration robustness and overall reliability. Process and structural improvements in the microconnect as well as the underlying diffusion barrier should also be further explored.

By comparing the electromigration test results of Cu-Sn micropads to Cu interconnect and solder bumps, data indicate the Cu–Sn microconnects have distinct failure mechanisms. It has been reported that the electromigration of Cu interconnect occurs predominantly by diffusion of Cu atoms along the interfaces and especially along the Cu/dielectric interface at the upper surface of an inlaid Cu interconnect [24]. The resulting failures are typically observed to be voids in Cu vias. This type of failure is reported to have an activation energy of 0.9 eV in Cu electromigration testing [23]. For electromigration-induced Cu interconnect voids which are caused by Cu drifting from electron flow, the activation energy usually ranges from 1.1 to 1.4 eV. [14] For solder bumps, the main reliability issues are current crowding and Joule heating, and the failure site often occurs at the under bump metallization (UBM). The activation energy is usually 0.64-1.07 eV for a SnAg solder bump with Cu UBM [13]. In this study, the intrinsic activation energies of Cu-Sn microconnects is measured to be 0.87-1.02 eV. By comparing the cross-sections of the electromigration tested samples having different failure modes, it is found that both Cu/ barrier interface and Cu/Cu–Sn drifting play important roles during the electromigration process. Current crowding may also play a role given the geometry.

# 5. Conclusions

In this paper, the electromigration performance of Cu-Sn microconnects in 3D ICs is investigated and the failure mechanisms are discussed. Electromigration properties of the microconnects are also compared with inlaid last metal Cu interconnects and Pb-free Sn-Cu solder bumps. After thermo-compression bonding of a two-die 3D IC test chip to form Cu-Sn microconnect die-to-die chains and Kelvin test structures, electromigration experiments are performed in both air and nitrogen ambient from 175 °C to 350 °C. For microconnect chain structures, the mean time to failure (MTTF) is longer for the die tested in N<sub>2</sub> ambient than in air. The results obtained in air show very little thermal activation between 300 °C and 350 °C, whereas the results obtained in N<sub>2</sub> show clear thermal activation. In both the electromigration stressed samples and the thermally stressed samples, migration of Cu to the sides of the microconnect are observed. The failed electromigration stressed Kelvin structures show voiding in both the microconnects and in the associated last metal connections to the microconnects.

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#### References

- P. Gueguen, C. Ventosa, L. Di Cioccio, H. Moriceau, F. Grossi, M. Rivoire, P. Leduc, L. Clavelier, Microelectron. Eng. 87 (3) (2010) 477–484.
- [2] S. Pozder, A. Jain, R. Chatterjee, Z. Huang, R.E. Jones, E.Acosta, B. Marlin, G. Hillmann, M. Sobczak, G. Kreindl, S. Kanagavel, H. Kostner, S. Pargfrieder, 3D Die-to-wafer Cu/Sn Microconnects Formed Simultaneously with an Adhesive Dielectric Bond Using Thermal Compression Bonding, in: 2008 International Interconnect Technology Conference, IEEE, 2008, pp. 46–48, http://dx.doi.org/ 10.1109/IITC.2008.4546921.
- [3] S. Pozder, A. Jain, R. Jones, Z. Huang, P. Justison, R. Chatterjee, P.S. Ho, E. Zschech, S. Ogawa, AIP Conf. Proc. 1143 (1) (2009) 213–223.

- [4] C.-T. Ko, K.-N. Chen, Microelectron. Reliab. 50 (4) (2010) 481-488.
- [5] S.M. Alam, R.E. Jones, S. Pozder, R. Chatterjee, S. Rauf, A. Jain, IEEE Trans. Very Large Scale Integr. Syst. 18 (3) (2010) 450–460.
- [6] S.M. Alam, R.E. Jones, S. Pozder, A. Jain, Die/wafer stacking with reciprocal design symmetry (RDS) for mask reuse in three-dimensional (3D) integration technology, in: 2009 10th International Symposium on Quality of Electronic Design, IEEE, 2009, pp. 569–575, http://dx.doi.org/10.1109/ISQED.2009. 4810357.
- [7] J.R. Black, IEEE Trans. Electron Devices 16 (4) (1969) 338-347.
- [8] A.G. Sabnis, VLSI electronics: microstructure science, Academic Press Ltd., (1990) [Online]. Available from: <a href="http://books.google.com/books/about/VLSI\_electronics.html?id=WCITAAAAMAAJ">http://books.google.com/books/about/VLSI\_electronics.html?id=WCITAAAAMAAJ</a>>.
- [9] K.N. Tu, Microelectron. Reliab. 51 (3) (2011) 517–523.
- [10] B.H.-L. Chao, X. Zhang, S.-H. Chae, P.S. Ho, Microelectron. Reliab. 49 (3) (2009) 253–263.
- [11] D.-Q. Yu, T.C. Chai, M.L. Thew, Y.Y. Ong, V.S. Rao, L.C. Wai, J.H. Lau, Electromigration study of 50 µm pitch micro solder bumps using four-point Kelvin structure, in: 2009 59th Electronic Components and Technology Conference, IEEE, 2009, pp. 930–935, http://dx.doi.org/10.1109/ECTC.2009. 5074124.
- [12] T.H. Lin, R.D. Wang, M.F. Chen, C.C. Chiu, S.Y. Chen, T.C. Yeh, L.C. Lin, S.Y. Hou, J.C. Lin, K.H. Chen, S.P. Jeng, D.C.H. Yu, Electromigration study of micro bumps at Si/Si interface in 3DIC package for 28nm technology and beyond, in: 2011 IEEE 61st Electronic Components and Technology Conference (ECTC), IEEE, 2011, pp. 346–350, http://dx.doi.org/10.1109/ECTC.2011.5898536.
- [13] S.-Y. Huang, C.-J. Zhan, Y.-W. Huang, Y.-M. Lin, C.-W. Fan, S.-C. Chung, K.-S. Kao, J.-Y. Chang, M.-L. Wu, T.-F. Yang, J. H. Lau, T.-H. Chen, Effects of UBM structure/material on the reliability performance of 3D chip stacking with 30µm-pitch solder micro bump interconnections, in: 2012 IEEE 62nd Electronic Components and Technology Conference, IEEE, 2012, pp. 1287–1292, http://dx.doi.org/10.1109/ECTC.2012.6249001.
- [14] R. Labie, P. Limaye, K. Lee, C. Berry, E. Beyne, I. De Wolf, Reliability testing of Cu-Sn intermetallic micro-bump interconnections for 3D-device stacking, in: 3rd Electronics System Integration Technology Conference ESTC, IEEE, 2010, pp. 1–5, http://dx.doi.org/10.1109/ESTC.2010.5642925.
- [15] Y. Wang, S.-H. Chae, R. Dunne, Y. Takahashi, K. Mawatari, P. Steinmann, T. Bonifield, T. Jiang, J. Im, P. S. Ho, Effect of intermetallic formation on electromigration reliability of TSV-microbump joints in 3D interconnect, in:

2012 IEEE 62nd Electronic Components and Technology Conference, IEEE, 2012, pp. 319–325, http://dx.doi.org/10.1109/ECTC.2012.6248849.

- [16] Q. Li, Y.C. Chan, S. Ismathullakhan, Growth characteristic study of intermetallic compounds growth in nanoscale-thickness Cu/Sn/Cu sandwich structure, in: 2011 IEEE 13th Electronics Packaging Technology Conference, IEEE, 2011, pp. 289–293, http://dx.doi.org/10.1109/EPTC.2011.61844433.
- [17] S.L. Wright, C.K. Tsang, J. Maria, B. Dang, R. Polastre, P. Andry, J. Knickerbocker, Micro-interconnection reliability: Thermal, electrical and mechanical stress, in: 2012 IEEE 62nd Electronic Components and Technology Conference, IEEE, 2012, pp. 1278–1286, http://dx.doi.org/10.1109/ECTC.2012.6249000.
- [18] Y.-M. Lin, C.-J. Zhan, J.-Y. Juang, J. H. Lau, T.-H. Chen, R. Lo, M. Kao, T. Tian, K.-N. Tu, Electromigration in Ni/Sn intermetallic micro bump joint for 3D IC chip stacking, in: 2011 IEEE 61st Electronic Components and Technology Conference (ECTC), IEEE, 2011, pp. 351–357, http://dx.doi.org/10.1109/ECTC. 2011.5898537.
- [19] F.-Y. Ouyang, H. Hsu, Y.-P. Su, T.-C. Chang, J. Appl. Phys. 112 (2) (2012) 023505.
- [20] S. Pozder, R. Chatterjee, A. Jain, Z. Huang, R.E. Jones, E. Acosta, Progress of 3D Integration Technologies and 3D Interconnects, in: 2007 IEEE International Interconnect Technology Conferencee, IEEE, 2007, pp. 213–215, http:// dx.doi.org/10.1109/IITC.2007.382393.
- [21] J. Li, J.W. Mayer, E.G. Colgan, J. Appl. Phys. 70 (5) (1991) 2820.
- [22] E.G. Liniger, C. Dziobkowski, Thin Solid Films 513 (1-2) (2006) 295-299.
- [23] Y. Hayashi, N. Matsunaga, M. Wada, S. Nakao, K. Watanabe, S. Kato, A. Sakata, A. Kajita, H. Shibata, Impact of oxygen on Cu surface for highly reliable low-k/ Cu interconnects with CuSiN and Ti-based barrier metal, in: Proc. IEEE International Interconnect Technology Conference, 2010, Burlingame, CA, IEEE, http://dx.doi.org/10.1109/IITC.2010.5510456.
- [24] S. Konishi, M. Moriyama, M. Murakami, Mater. Trans. 43 (2002) 1624-1628.
- [25] C.W. Park, R.W. Vook, Appl. Phys. Lett. 59 (2) (1991) 175.
- [26] M.H. Tsai, W.J. Tsai, S.L. Shue, C.H. Yu, M.S. Liang, Reliability of dual damascene Cu metallization, in: Proc. IEEE International Interconnect Technology Conference, IEEE, 2000, pp. 214–216, http://dx.doi.org/10.1109/IITC.2000. 854329.
- [27] M. Lu, D.-Y. Shih, C. Goldsmith, T. Wassick, Comparison of electromigration behaviors of SnAg and SnCu solders, in: IEEE International Reliability Physics Symposium, IEEE, 2009, pp. 149–154, http://dx.doi.org/10.1109/IRPS.2009. 5173241.