Experimental and Numerical Investigation of Interdie Thermal Resistance in Three-Dimensional Integrated Circuits

Leila Choobineh
Mem. ASME
Mechanical Engineering,
SUNY Polytechnic Institute,
100 Seymour Road,
Utica, NY 13502
e-mail: Leila.choobineh@sunyit.edu

Jared Jones
Mechanical and Aerospace Engineering,
University of Texas at Arlington,
500 W First Street, Room 211,
Arlington, TX 76019

Ankur Jain
Mem. ASME
Mechanical and Aerospace Engineering,
University of Texas at Arlington,
500 W First Street, Room 211,
Arlington, TX 76019
e-mail: jaina@uta.edu

Three-dimensional integrated circuits (3D ICs) attract much interest due to several advantages over traditional microelectronics design, such as electrical performance improvement and reducing interconnect delay. While the power density of 3D ICs increases because of vertical integration, the available substrate area for heat removal does not change. Thermal modeling of 3D ICs is important for improving thermal and electrical performance. Experimental investigation on the thermal measurement of 3D ICs and determination of key physical parameters in 3D ICs thermal design are curtail. One such important parameter in thermal analysis is the interdie thermal resistance between adjacent die bonded together. This paper describes an experimental method to measure the value of interdie thermal resistance between two adjacent dies in a 3D IC. The effect of heating one die on the temperature of the other die in a two-die stack is measured over a short time period using high-speed data acquisition to negate the effect of boundary conditions. Numerical simulation is performed and based on a comparison between experimental data and the numerical model, the interdie thermal resistance between the two dies is determined. A theoretical model is also developed to estimate the value of the interdie thermal resistance. Results from this paper are expected to assist in thermal design and management of 3D ICs. [DOI: 10.1115/1.4036404]

Introduction

Three-dimensional integrated circuits (3D ICs) are fabricated by stacking multiple devices or die together and making interconnection between them [1,2]. There are several advantages of 3D ICs compared to traditional two-dimensional ICs. For example, the overall system performance increases along with a reduction in system size [3]. It has also been shown that electrical performance parameters such as frequency, delay, power consumption, and interconnect bandwidth can be improved through chip-level 3D integration [4,5].

Higher density and smaller interlayer connection dimensions are key process elements to optimize 3D ICs. Several manufacturing and design methods of 3D circuits, such as wafer level stacking, chip to chip stacking, and bottom up and top down fabrication, have been explored, and the specifications of every method have been analyzed [6–8]. Even though 3D IC technology results in reduced interconnect length, removing heat from such architectures has proven to be difficult. Different liquid- and solid-state cooling systems have been explored to reduce hot spot and junction temperature [9–11]. Several studies on the effect of copper-filled through silicon vias (TSVs) for electrical connection, as well as thermal dissipation, in 3D-stacked chips have been performed numerically and experimentally [12–15].

While the power density of a 3D IC is dramatically higher due to vertical integration, the substrate area available for heat removal does not significantly change [16]. A direct result of this is that 3D ICs are expected to experience significant temperature rise, and thermal management becomes an important design consideration. The importance of thermal management of 3D ICs has been recognized [17–20], and several studies have been done numerically and analytically to predict the temperature field in 3D-stacked chips [21–32]. From a heat transfer perspective, a 3D IC is a multilayer structure with heat generation in each stratum [33]. Steady-state heat conduction in multilayer bodies has been studied analytically [33–37]. Early works in this field considered the thermal performance of a 3D IC based on a thermal resistance network [33]. More sophisticated models, including those based on analytical solutions for the temperature field, have been developed [27–29]. Numerical thermal analysis of 3D ICs has been done [38] for a better understanding of the nature of heat transfer in a 3D IC. Regardless of the method used in the computational and analytical method, these models should be validated against experimental measurement. Thus, several experimental works on the thermal measurement of 3D ICs have been done [39,40]. Experimental measurement of the thermal performance of a two-die stack has been presented. However, the measurements were limited only to the die performance. Thus, the effect of interconnection on thermal performance has not yet been considered [41].

Some interdie thermal resistance exists between two adjacent dies in a 3D stack depending on the nature of the integration [39,40,42]. Some part of the interdie thermal resistance occurs because of the connection methods between two adjacent dies such as metal pillars and underfill materials around the metal pillars. This interdie thermal resistance would affect the thermal characteristic of the package [43,44]. In addition, the die attachment quality and thermal resistance need to be controlled in order to avoid high thermal resistance and overheating of every die that may ruin the device [16,43,44]. Since the interdie thermal resistance is one of the important key design parameters, and it affects thermal performance of the package, experimental measurements in order to determine interdie thermal resistance between the two dies are crucial.

Several experimental investigations have been carried out to determine interdie thermal resistance in 3D-stacked packages. Thermal performance of a package with multiple dies has been explored numerically, and the effect of different die configurations on the thermal simulation has been analyzed. In this work,

Contributed by the Electronic and Photonic Packaging Division of ASME for publication in the JOURNAL OF ELECTRONIC PACKAGING. Manuscript received December 16, 2016; final manuscript received March 27, 2017; published online June 12, 2017. Assoc. Editor: Justin A. Weibel.

 Copyright © 2017 by ASME

Downloaded From: http://electronicpackaging.asmedigitalcollection.asme.org/pdfaccess.ashx?url=/data/journals/jepae4/936184/ on 06/19/2017 Terms of Use: http://www.asme.o

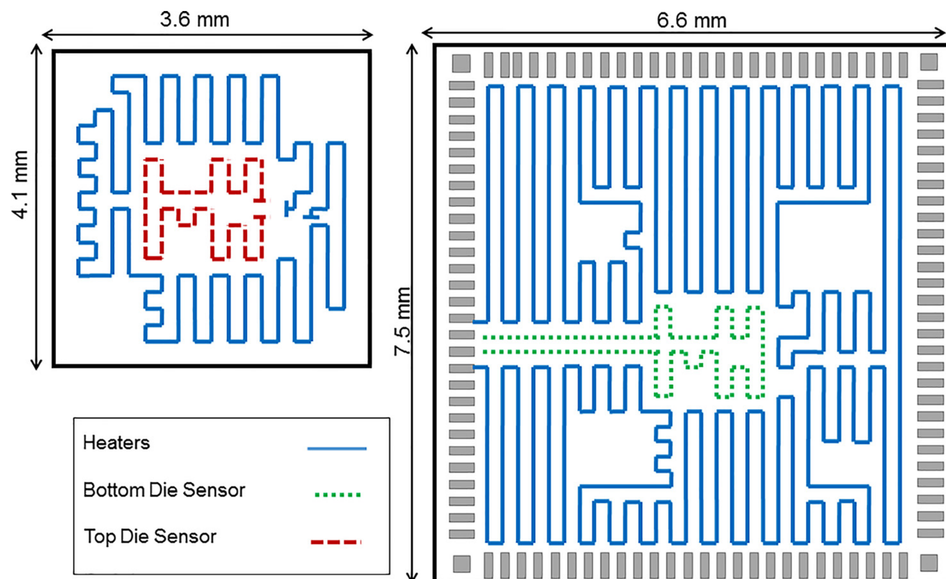

Fig. 1 Schematic of the two dies in the 3D IC. Blue lines show the heater, red lines show the top die sensor, and green lines show the bottom die sensor (see color figure online).

heat transfer is considered to be one-dimensional, and also, the effect of convective heat transfer is neglected, which may not be realistic. Furthermore, the total thermal resistance between junctions and ambient has been calculated, while the effect of thermal resistance of every attachment on the thermal performance has not been considered [45]. In another study, microbump thermal resistance in a four-layer chip stack has been measured experimentally with and without underfill materials and the effect of microbump pitches on the thermal resistance has been investigated [40]. The experimental setup and measurement model used in the study are applicable in thermal measurements of 3D ICs; however, the experimental results have not been validated against numerical simulation or theoretical model. In another study, the temperature distribution in a 3D IC has been measured experimentally and it has been used to determine the equivalent thermal conductivity of the chip; however, each layer was not studied separately [42].

In this paper, an experimental technique to measure the interdie thermal resistance of a two-die stack is presented which can be helpful in determining the interdie thermal resistance of 3D ICs with more than two stacked die and interposer-based systems (2.5D ICs). First, the numerical simulation has been conducted and the results demonstrate the influence of interdie thermal resistance on both steady-state and transient thermal conduction in a two-die 3D ICs sample. Then, the experimental setup to measure interdie thermal resistance is presented, which is based on heating one die and measuring temperature rise in the other die in a short period of time to rule out boundary effects in the experimental setup. This technique can be used to determine the interdie thermal resistance between the two dies or thermal resistance of every die. The theoretical model developed and the experimental data compared well with experimental results.

Experimental Setup

The 3D IC used in this work is a two-die stack consisting of two unequally sized die. The bottom die is 6.6 mm × 7.5 mm, and the top die is 4.1 mm × 3.6 mm. Both dies have 0.25 mm thickness and are connected to each other by face-to-face bonding of copper pillars on the top faces of both dies. Each die contains an embedded heater and a resistance thermometry-based temperature sensor, as shown in Fig. 1. The heater and sensor on each die are accessible by input and output (I/O) pads located on the periphery of the bottom die. Sensors are located approximately at the center of each die, and the embedded heaters are serpentine structures that cover the entire die in a nearly uniform fashion.

First, the two-die stack is glued on a leadless chip carrier (LCC). Then, in order to access I/O pads, gold wire bonds are made between I/O pads on the periphery of the bottom die and LCC contact pads. Since the size of the LCC pads is smaller than typical bond wire diameter, and it is impossible to access the LCC pads by regular solder wiring, the LCC substrate is mounted on a compatible pin socket and electrical wires are soldered to the socket leads. Ultimately, it is possible to access every heater and sensor on every die through I/O pads on the periphery of the bottom die, gold wire bonding, LCC pads, socket pins, and finally soldered wires. A picture of the entire package is shown in Fig. 2.

Results and Discussion

In every multichip stack, some interdie thermal resistance exists between adjacent die because of the connection methods, such as metal pillars with interdie materials. The amount of interdie thermal resistance between adjacent die in a 3D-stacked die structure influences the temperature rise in every layer and thermal characteristics of the package.

Numerical simulation has been carried out by using ANSYS CFX for the introduced two-die stack. In Fig. 3, the temperature rise in

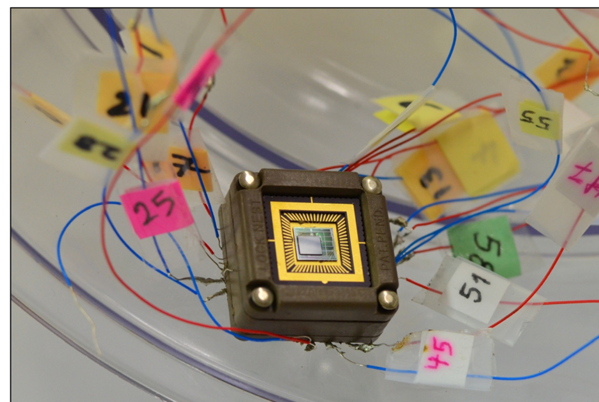

Fig. 2 The substrate mounted in the socket and soldered wires

Downloaded From: http://electronicpackaging.asmedigitalcollection.asme.org/pdfaccess.ashx?url=/data/journals/jepae4/936184/ on 06/19/2017 Terms of Use: http://www.asme.o

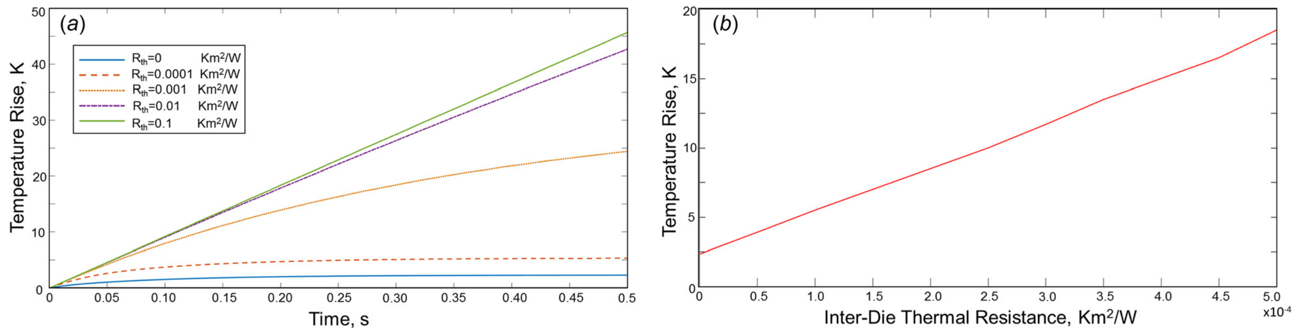

Fig. 3 (*a*) Temperature rise in bottom die sensor versus time in the two-die stack for different amounts of thermal resistance between the two dies and (*b*) steady-state temperature rise in BDS for different amounts of thermal resistance between the two dies by applying 100 mA current (0.6 W power) in top die heater

Table 1 Steady-state temperature rise in bottom die sensor for different amounts of thermal resistance between the two dies by applying 100 mA current (0.6 W power) in top die heater

Interdie thermal resistance (km^2/W)	Temperature rise in bottom die sensor (K)
0.00000	2.3
0.00001	2.7
0.00005	3.9
0.00010	5.5
0.00015	7.0
0.00020	8.5
0.00025	10.0
0.00030	11.7
0.00035	13.5
0.00040	15.0
0.00045	16.5
0.00050	18.5

Table 2 Transient temperature rise in bottom die sensor for different amounts of interdie thermal resistance between the two dies by applying 100 mA current (0.6 W power) in top die heater at time 0.5 s

Interdie thermal resistance (km^2/W)	Temperature rise in bottom die sensor (K)
0.0	0.5
0.0001	1.1
0.001	4.9
0.01	8.5
0.1	9.1

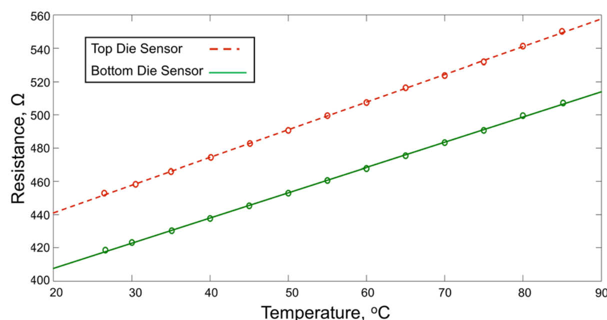

Fig. 4 Thermal calibration curve for top and bottom die sensors

the bottom die sensor is plotted by applying different amounts of thermal resistance between the two dies when 100 mA current (0.6 W power) passes through the top die heater. The numerical simulation results have been provided in Tables 1 and 2. The plots show an increase in the temperature rise in the bottom die sensor as interdie thermal resistance increases for both steady-state and transient thermal conduction in the two-die stack. These results from the numerical simulations demonstrate the importance of understanding the amount of interdie thermal resistance in every multichip package in order to have precise thermal modeling of the 3D IC and better engineering of the interdie interfaces to reduce the interdie thermal resistance which aids in reducing the temperature rise in micropackages. Because of the importance of the interdie thermal resistance on the thermal management of 3D ICs, an experimental measurement model is introduced and the two-die stack is used for the measurements.

In order to measure the interdie thermal resistance experimentally, calibration is carried out by measuring the resistance of each sensor and heater at several temperatures between 20 °C and 90 °C in 5 °C increments. A waiting period of 30 mins is implemented at each temperature to eliminate transient thermal effects. A test current of only 10 μA is used to minimize self-heating.

The thermal calibration results for thermal sensors are shown in Fig. 4. Experimentally measured data are shown in circles, and a linear fit was performed showing an accurate fit. Since the electrical resistance of metals increases linearly with temperature, the plots trends are reasonable.

The slope of the curve shows the temperature coefficient of resistivity that is 0.00374 $^\circ$C^{-1} and 0.00369 $^\circ$C^{-1} for the top and bottom die sensors, respectively. This has good agreement with the standard value of thermal coefficient of resistivity of aluminum (0.004 $^\circ$C^{-1}). The experimental value of temperature coefficient of resistivity for the top die and bottom die heaters is measured with the same method and they are 0.00389 $^\circ$C^{-1} and 0.00347 $^\circ$C^{-1}, respectively. The experimentally determined temperature coefficient of resistivity of every heater and sensor was used to calculate the temperature rise in every heater and sensor from electrical resistance rise measurements during actual experiments.

A finite element simulation based model is developed in order to investigate interdie thermal resistance between adjacent die in the geometry representative of the experimental test device. The semi-infinite domain assumption can be applied to the thermal conduction in the top die and bottom die domains. The assumption is valid as long as the thermal penetration depth (D_{th}) in the experiment duration time (time_{Exp}) is much smaller than the thickness of the top die and the bottom die [46]

$$D_{\text{th}} = 2\sqrt{\alpha \cdot \text{time}_{\text{Exp}}} \ll W_T \qquad (1)$$

where α is the thermal diffusivity of silicon which every die is fabricated from. For a given geometry where W_{T} (top die thickness)

Downloaded From: http://electronicpackaging.asmedigitalcollection.asme.org/pdfaccess.ashx?url=/data/journals/jepae4/936184/ on 06/19/2017 Terms of Use: http://www.asme.o

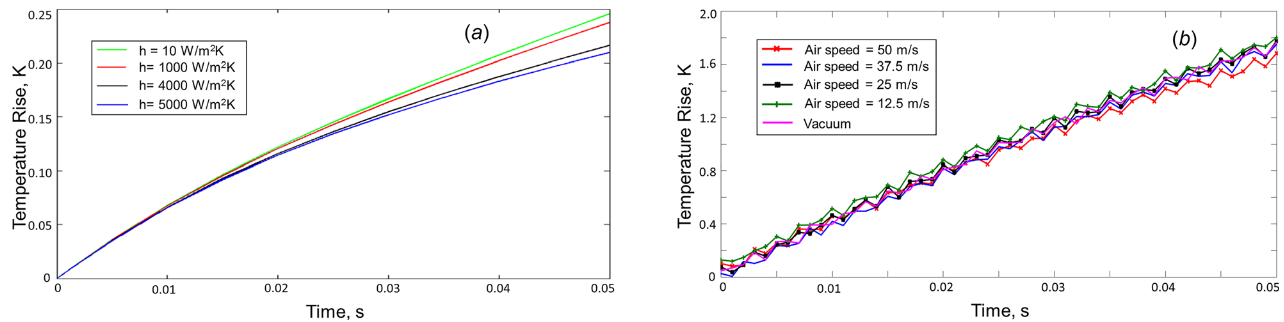

Fig. 5 The temperature rise in the bottom die sensor versus time by heating the top die for different values of coefficient of convective heat transfer: (*a*) finite element simulation and (*b*) experimental data

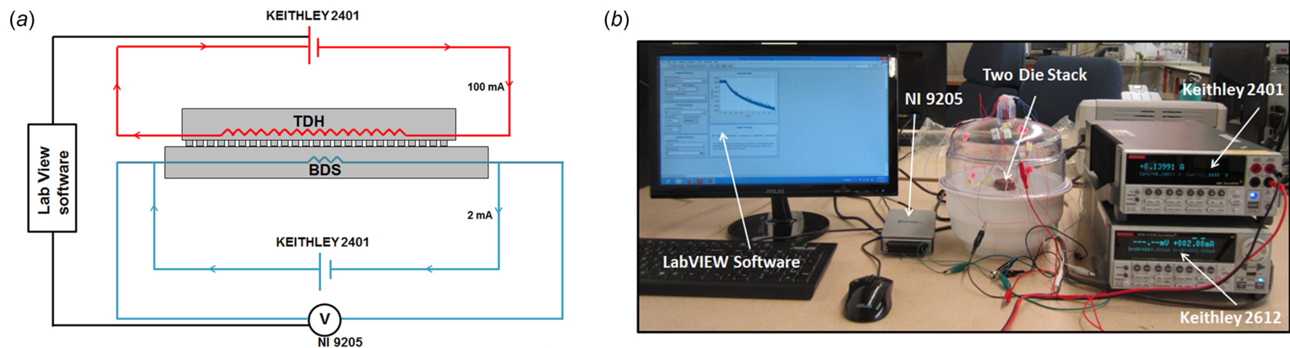

Fig. 6 Experimental setup for measuring the interdie thermal resistance between the two dies

is known, the semi-infinite domain assumption is valid, as long as the duration of experiment (time_{Exp}) satisfies

$$\text{time}_{\text{Exp}} \ll \frac{W_T^2}{4\alpha} \tag{2}$$

Using the semi-infinite assumption for the geometry means that the boundary conditions will not affect the temperature rise in every die within the experimental time of time_{Exp}. The calculation shows that when the duration of the experiment is less than 25 ms for this device, the semi-infinite assumption can be applied to the geometry. Therefore, the convective boundary condition does not affect the temperature rise profile.

In order to validate the semi-infinite assumption, the finite element simulation has been carried out by using commercial software ANSYS CFX. Temperature rise as a function of time is determined for different values of the convective heat transfer coefficient. The results presented in Fig. 5(*a*) show that for the first 25 ms, the temperature rise in the two-die stack does not depend on the convective heat transfer coefficient and the effect of convective boundary condition can be neglected. In addition, the experimental measurement has been done by passing 100 mA direct current (0.6 W power) through the top die heater and measuring the corresponding temperature rise in the bottom die sensor. Air has been blown around the device during the experiment causing a change in the value of the convective heat transfer coefficient relative to the air speed. Note that some fluctuation happens because of inaccuracy and noise in measurement equipment. The experimental data presented in Fig. 5(*b*) show the independency of temperature rise to the convective heat transfer coefficient for the first 25 ms, which confirms the simulation results and semi-infinite domain assumption. This performance can be used to determine the interdie thermal resistance between two adjacent die in the two-die stack.

Keithley 2401 and Keithley 2612 are used for supplying current to the heater and sensor, respectively, and NI 9205 is programed by LABVIEW to measure voltage in the sensor. High-speed data acquisition was done every microsecond according to the experimental setup shown in Fig. 6.

Power is generated in one die by increasing the direct current in the heater, and the temperature rise in every sensor is calculated by converting the voltage rise of every sensor to a corresponding temperature rise using the temperature coefficient of resistivity of every sensor found from calibration results. For the same geometry, for a given value of power in one die, the transient finite element simulation was carried out by using the commercial software, ANSYS, and different values of interdie thermal resistance have been applied between the two dies. In order to determine interdie thermal resistance between the two dies, the simulation temperature rise in one sensor was plotted and compared with the equivalent experimental temperature rise plot. The value of interdie thermal resistance that the finite element results match well with the experimental curve is the value of interdie thermal resistance. The comparison of finite element simulation and experimental data for different cases, as shown in Figs. 7(*a*) and 7(*b*), indicates that the experimental value of interdie thermal resistance is about 1.0 μ km^2/W.

A theoretical model has been developed to validate the experimental results. Copper pillars are utilized between the two dies for attachment, and the underfill material is considered to be air. The geometry of the copper pillar arrays between the two dies has been shown in Fig. 8. Because of the symmetry of the geometry, only one copper-air cell has been used for the calculations. Thermal conductivities are set as the bulk thermal conductivities that are 401 W/m K and 0.0257 W/m K for copper and air, respectively.

Since copper and air thermal resistances are in parallel, the overall thermal resistance, which is equivalent to the interdie thermal resistance, is found by applying Eq. (3). The calculated theoretical value of interdie thermal resistance is 0.735 μ km^2/W, which is similar to the value obtained from the experimental measurements.

Downloaded From: http://electronicpackaging.asmedigitalcollection.asme.org/pdfaccess.ashx?url=/data/journals/jepae4/936184/ on 06/19/2017 Terms of Use: http://www.asme.o

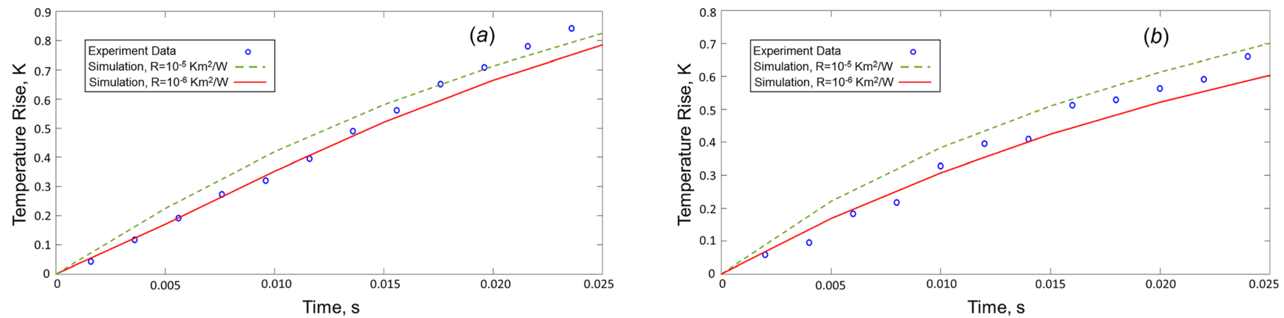

Fig. 7 (*a*) Measured temperature rise in bottom die sensor (BDS) due to 100 mA current (0.6 W power) in top die heater (TDH) and (*b*) measured temperature rise in top die sensor (TDS) due to 80 mA current (0.37 W power) in bottom die heater (BDH)

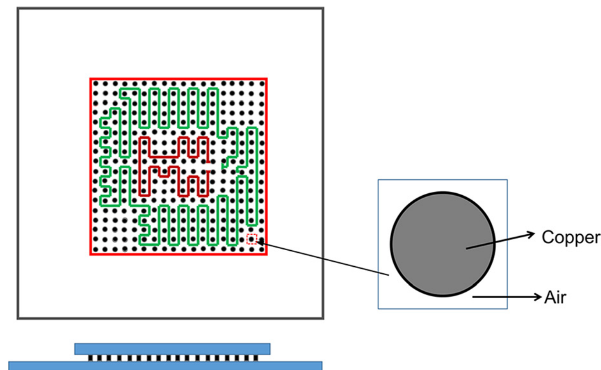

Fig. 8 The geometry of copper pillars used to make attachment between the two dies

$$R = \frac{L}{kA} \tag{3}$$

$$\frac{1}{R_{\text{total}}} = \frac{1}{R_{\text{Copper}}} + \frac{1}{R_{\text{Air}}} \tag{4}$$

Note that some deviation between the experimentally measured value of thermal resistance and theoretical results is to be expected. The deviation is expected because the thermophysical properties of materials deviate from standard bulk values, assuming air as underfill material, imperfect bonding between the metal pillars and every die, and inaccuracy in measurement equipment.

Interdie thermal resistance is dependent on the metal pillars design and thermal properties of metal pillars and underfill material. Interdie thermal resistance decreases by increasing the thermal conductivity of metal pillars and underfill materials, which leads to lower temperature rise in the system. Copper with high thermal conductivity and thermally conductive underfill materials can be suitable choices for interconnecting layers to reduce interdie thermal resistance, which ultimately results in more thermal friendly design.

Conclusion

This paper discusses an experimental method to measure the interdie thermal resistance between adjacent die in 3D ICs. Numerical simulation has been performed by using ANSYS CFX to study thermal conduction in a two-die stack 3D IC when one die is generating heat. The numerical results demonstrate the effect of interdie thermal resistance between the two dies on the temperature rise of the other die. In order to measure interdie thermal resistance experimentally, the temperature rise of every die was measured by using a high-speed data-acquisition technique performed through LABVIEW. A numerical model was also developed to predict the temperature distribution in the same geometry, with consideration of different amounts of interdie thermal resistance. Then, by comparing the experimental data with numerical simulation, the value of interdie thermal resistance was found. The results from this paper may be useful in determining the interdie thermal resistance between adjacent die in 3D ICs and assist in the understanding of thermal transport in 3D ICs enabling friendlier thermal designs of a new generation of 3D ICs.

Acknowledgment

This material is based upon the work supported by the National Science Foundation under Grant No. CBET-1236370.

References

[1] Banerjee, K., Souri, S. J., and Saraswat, K. C., 2001, "3-D ICs: A Novel Chip Design for Improving Deep Submicron Interconnect Performance and Systems-on-Chip Integration," Proc. IEEE, **89**(5), pp. 602–633.
[2] Patti, R., 2006, "Three-Dimensional Integrated Circuits and the Future of System-on-Chip Designs," Proc. IEEE, **94**(6), pp. 1214–1224.
[3] Beyne, E., 2006, "3D System Integration Technologies," International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA-Tech), Hsinchu, Taiwan, Apr. 24–26, pp. 1–9.
[4] Said, F., Abbott, D., and Franzon, P. D., 1998, "A Review of 3-D Packaging Technology," IEEE Trans. Compon. Packag. Manuf. Technol. Part B, **21**(1), pp. 2–14.
[5] Knickerbocker, J. U., Andry, P. S., Dang, B., Horton, R. R., Patel, C. S., Polastre, R. J., Sakuma, K., Sprogis, E. S., Tsang, C. K., Webb, B. C., and Wright, S. L., 2008, "3D Silicon Integration," 58th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 538–543.
[6] Chan, V. W. C., Chan, P. C. H., and Chan, M., 2001, "Three-Dimensional CMOS SOI Integrated Circuit Using High Temperature Metal-Induced Lateral Crystallization," IEEE Trans. Electron Devices, **48**(7), pp. 1394–1399.
[7] Topol, A. W., La Tulipe, D. C., Shi, L., Frank, D. J., Bernstein, K., Steen, S. E., Kumar, A., Singco, G. U., Young, A. M., Guarini, K. W., and Leong, M., 2006, "Three-Dimensional Integrated Circuits," IBM J. Res. Dev., **50**(4/5), pp. 491–506.
[8] Guarini, K. W., Topol, A. T., Leong, M., Yu, R., Shi, L., Newport, M. R., Frank, D. J., Singh, D. V., Cohen, G. M., Nitta, S. V., Boyd, D. C., O'Neil, P. A., Tempest, S. L., Pogge, H. B., Purushothaman, S., and Haensch, W. E., 2002, "Electrical Integrity of State-of-the-Art 0.13l m SOI CMOS Devices and Circuits Transferred for Three-Dimensional (3D) Integrated Circuit (IC) Fabrication," International Electron Devices Meeting (IEDM) Technical Digest, San Francisco, CA, Dec. 8–11, p. 943.
[9] Brunschwiler, T., Michel, B., Rothuizen, H., Kloter, U., Wunderle, B., Oppermann, H., and Reichl, H., 2009, "Interlayer Cooling Potential in Vertically Integrated Packages," Microsyst. Technol., **15**(1), pp. 57–74.
[10] Schindler-Saefkow, F., Wittler, O., May, D., and Michel, B., 2006, "Thermal Management in a 3D-PCB-Package With Water Cooling," Electronics System-integration Technology Conference (ESTC), Dresden, Germany, Sept. 5–7, pp. 107–110.
[11] Sikka, K., Wakil, J., Toy, H., and Liu, H., 2012, "An Efficient Lid Design for Cooling Stacked Flip-Chip 3D Packages," 13th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM), San Diego, CA, May 30–June 1, pp. 606–611.
[12] Cong, J., Luo, G., Wei, J., and Zhang, Y., 2007, "Thermal-Aware 3D IC Placement Via Transformation," Asia and South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, Jan. 23–26, pp. 780–785.

Downloaded From: http://electronicpackaging.asmedigitalcollection.asme.org/pdfaccess.ashx?url=/data/journals/jepae4/936184/ on 06/19/2017 Terms of Use: http://www.asme.o

[13] Goplen, B., and Sapatnekar, S. S., 2006, "Placement of Thermal Vias in 3D ICs Using Various Thermal Objectives," IEEE Trans. Comput. Aided Des. Integr. Circuits Syst., **26**(4), pp. 692–709.
[14] Savidis, I., Alam, S., Jain, A., Pozder, S., Jones, R. E., and Chatterjee, R., 2010, "Electrical Modeling and Characterization of Through-Silicon Vias (TSVs) for 3D Integrated Circuits," Microelectron. J., **41**(1), pp. 9–16.
[15] Pi, Y., Wang, W., and Jin, Y., 2016, "An Accurate Calculation Method on Thermal Effectiveness of TSV and Wire," IEEE 18th Electronics Packaging Technology Conference (EPTC), Singapore, Nov. 30–Dec. 3, pp. 569–573.
[16] Rencz, M., 2005, "Thermal Issues in Stacked Die Packages," 21st Annual IEEE Semiconductor Thermal Measurement and Management Symposium (STHERM), San Jose, CA, Mar. 15–17, pp. 307–312.
[17] Link, G. M., and Vijaykrishnan, N., 2006, "Thermal Trends in Emerging Technologies," 7th International Symposium on Quality Electronic Design (ISQED), San Jose, CA, Mar. 27–29, pp. 625–632.
[18] Loi, G. L., Agrawal, B., Srivastava, N., Lin, S.-C., Sherwood, T., and Banerjee, K., 2006, "A Thermally-Aware Performance Analysis of Vertically Integrated (3-D) Processor-Memory Hierarchy," 43rd ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, July 24–28, pp. 991–996.
[19] Das, S., Chandrakasan, A., and Reif, R., 2004, "Timing, Energy, and Thermal Performance of Three Dimensional Integrated Circuits," 14th ACM Great Lakes Symposium on VLSI, Boston, MA, Apr. 26–28, pp. 338–343.
[20] Yan, H., Zhou, Q., and Hong, X., 2009, "Thermal Aware Placement in 3D ICs Using Quadratic Uniformity Modeling Approach," Integr. VLSI J., **42**(2), pp. 175–180.
[21] Kleiner, M. B., Kuhn, S. A., Ramm, P., and Weber, W., 1995, "Thermal Analysis of Vertically Integrated Circuits," International Electron Devices Meeting (IEDM) Technical Digest, Libertyville, IL, Dec. 10–13, pp. 487–490.
[22] Chiang, T.-Y., Souri, S. J., Chui, C. O., and Saraswat, K. C., 2001, "Thermal Analysis of Heterogeneous 3-D ICs With Various Integration Scenarios," International Electron Devices Meeting (IEDM) Technical Digest, Washington, DC, Dec. 2–5, pp. 31.2.1–31.2.4.
[23] Haji-Sheikh, A., and Beck, J. V., 2002, "Temperature Solution in Multi-Dimensional Multi-Layer Bodies," Int. J. Heat Mass Transfer, **45**(9) pp. 1865–1877.
[24] Cong, J., Wei, J., and Zhang, Y., 2004, "A Thermal-Driven Floorplanning Algorithm for 3D ICs," IEEE/ACM International Conference on Computer Aided Design (ICCAD), San Jose, CA, Nov. 7–11, pp. 306–313.
[25] Geer, J., Desai, J., and Sammakia, B., 2007, "Heat Conduction in Multilayered Rectangular Domains," ASME J. Electron. Packag., **129**(4), pp. 440–451
[26] Ayala, J. L., Sridhar, A., and Cuesta, D., 2010, "Thermal Modeling and Analysis of 3D Multi-Processor Chips," Integr. VLSI J., **43**(4), pp. 327–341.
[27] Choobineh, L., and Jain, A., 2012, "Analytical Solution for Steady-State and Transient Temperature Field in Vertically Integrated Three-Dimensional Integrated Circuits (3D ICs)," IEEE Trans. Compon. Packag. Manuf. Technol., **2**(12), pp. 2031–2039.
[28] Choobineh, L., and Jain, A., 2013, "Determination of Temperature Distribution in Three-Dimensional Integrated Circuits (3D ICs) With Unequally-Sized Die," Appl. Therm. Eng., **56**(1), pp. 176–184.
[29] Choobineh, L., and Jain, A., 2015, "An Explicit Analytical Model for Rapid Computation of Temperature Field in a Three-Dimensional Integrated Circuit (3D IC)," Int. J. Therm. Sci., **87**, pp. 103–109.
[30] Dogruoz, M. B., 2016, "Assessment of Joule Heating and Temperature Distribution on Printed Circuit Boards Via Electrothermal Simulations," ASME J. Electron. Packag., **138**(2), p. 021004.
[31] Wang, N., Jin, Y., Pi, Y., and Wang, W., 2016, "A Full Chip Scale Numerical Simulation Method for Thermal Management of 3D IC," 17th International Conference on Electronic Packaging Technology (ICEPT), Wuhan, China, Aug. 16–19, pp. 690–693.
[32] Tavakkoli, F., Ebrahimi, S., Wang, S., and Vafai, K., 2016, "Thermophysical and Geometrical Effects on the Thermal Performance and Optimization of a Three-Dimensional Integrated Circuit," ASME J. Heat Transfer, **138**(8), p. 082101.
[33] Jain, A., Jones, R. E., Chatterjee, R., and Pozder, S., 2010, "Analytical and Numerical Modeling of the Thermal Performance of Three-Dimensional Integrated Circuits," IEEE Trans. Compon. Packag. Technol., **33**(1), pp. 56–63.
[34] Haji-Sheikh, A., Beck, J. V., and Agonafer, D., 2003, "Steady-State Heat Conduction in Multi-Layer Bodies," Int. J. Heat Mass Transfer, **46**(13), pp. 2363–2379.
[35] Rahman, A., and Reif, R., 2001, "Thermal Analysis of Three-Dimensional (3-D) Integrated Circuits (ICs)," IEEE International Interconnect Technology Conference (IITC), Burlingame, CA, June 4–6, pp. 157–159.
[36] Oprins, H., Cherman, V. O., Vandevelde, B., Van der Plas, G., Marchal, P., and Beyne, E., 2012, "Numerical and Experimental Characterization of the Thermal Behavior of a Packaged DRAM-on-Logic Stack," IEEE 62nd Electronic Components and Technology Conference (ECTC), San Diego, CA, May 29–June 1, pp. 1081–1088.
[37] Li, J.-F., and Wu, C.-W., 2010, "Is 3D Integration an Opportunity or Just a Hype?," 15th Asia and South Pacific Design Automation Conference (ASP-DAC), Taipei, Taiwan, Jan. 18–21, pp. 541–543.
[38] Puttaswamy, K., and Loh, G. H., 2006, "Thermal Analysis of a 3D Die-Stacked High-Performance Microprocessor," 16th ACM Great Lakes Symposium on VLSI (GLSVLSI), Philadelphia, PA, Apr. 30–May 1, pp. 19–24.
[39] Oprins, H., Cherman, V., Vandevelde, B., Torregiani, C., Stucchi, M., Van der-Plas, G., Marchal, P., and Beyne, E., 2011, "Characterization of the Thermal Impact of Cu-Cu Bonds Achieved Using TSVs on Hot Spot Dissipation in 3D Stacked ICs," Electronic Components and Technology Conference (ECTC), Lake Buena Vista, FL, May 31–June 3, pp. 861–868.
[40] Colgan, E. G., Andry, P., Dang, B., Magerlein, J. H., Maria, J., Polastre, R. J., and Wakil, J., 2012, "Measurement of Microbump Thermal Resistance in 3D Chip Stacks," 28th Annual IEEE Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), San Jose, CA, Mar. 18–22, pp. 1–7.
[41] Choobineh, L., Vo, N., Uehling, T., and Jain, A., 2013, "Experimental Measurement of the Thermal Performance of a Two-Die 3D Integrated Circuit (3D IC)," ASME Paper No. IPACK2013-73167.
[42] Matsumoto, K., Ibaraki, S., Sueoka, K., Sakuma, K., Kikuchi, H., Orii, Y., and Yamada, F., 2011, "Experimental Thermal Resistance Evaluation of a Three-Dimensional (3D) Chip Stack," 27th Annual IEEE Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), San Jose, CA, Mar. 20–24, pp. 125–130.
[43] Bozorg-Grayeli, E., Reifenberg, J. P., Asheghi, M., Wong, H. S. P., and Goodson, K. E., 2013, "Thermal Transport in Phase Change Memory Materials," Annu. Rev. Heat Transfer., **16**(1), pp. 397–428.
[44] Yovanovich, M., 2005, "Four Decades of Research on Thermal Contact, Gap, and Joint Resistance in Microelectronics," IEEE Trans. Compon. Packag. Technol., **28**(2), pp. 182–206.
[45] Joiner, B., Montes de Oca, J. A., and Neelakantan, S., 2009, "Measurement and Simulation of Stacked Die Thermal Resistances," IEEE Trans. Compon. Packag. Technol., **32**(4), pp. 709–715.
[46] Hahn, D. W., and Özisik, M. N., 2012, *Heat Conduction*, 3rd ed., Wiley, Hoboken, NJ.

Downloaded From: http://electronicpackaging.asmedigitalcollection.asme.org/pdfaccess.ashx?url=/data/journals/jepae4/936184/ on 06/19/2017 Terms of Use: http://www.asme.o