Analytical Solution for Steady-State and Transient Temperature Fields in Vertically Stacked 3-D Integrated Circuits

Leila Choobineh and Ankur Jain

Abstract-Vertical integration for microelectronics poses significant challenges related to dissipation of heat generated in multiple device planes. Thermal management of 3-D integrated circuits (3-D ICs) is recognized to be one of the foremost technological and research challenges currently blocking the widespread adoption of this promising technology. The computation of steady-state and transient temperature fields in a 3-D IC is critical for determining the thermal characteristics of a 3-D IC and for evaluating any candidate thermal management technology. This paper presents an analytical solution for the 3-D temperature field in a 3-D IC based on the solution of the governing energy equations using Fourier series expansion for steady-state temperature fields. In addition, this approach is combined with Laplace transforms to determine transient temperature fields. Comparison of the temperature fields predicted by the proposed models with finite-element simulations shows excellent agreement. The model is used to compute the temperature field in a representative 3-D IC, and it is shown that by utilizing a thermal-friendly floorplanning approach, the maximum temperature of the 3-D IC is reduced substantially.

Index Terms—3-D integrated circuits (3-D ICs), floorplanning, Fourier series expansion, Laplace transforms, thermal management.

I. INTRODUCTION

3-D INTEGRATED CIRCUITS (3-D ICs) technology is a promising approach for next-generation semiconductor microelectronics [1]–[3]. By stacking multiple silicon strata and interconnecting circuits on different strata using throughsilicon vias (TSVs) and metal micropads, it is possible to obtain significant electrical performance benefits without resorting to the prohibitively expensive alternative of dimensional scaling [2]. For example, significant reduction in signal transmission delay and interconnect power in 3-D ICs compared to traditional system-on-chip (SOC) technology has been demonstrated [4], [5]. In addition, 3-D IC technology enables compact integration of heterogeneous technologies and offers the exciting possibility of cost-effective manufacturing strategies such as differentiated technologies in various strata, recip-

Manuscript received January 20, 2012; revised July 25, 2012; accepted July 27, 2012. Date of publication November 12, 2012; date of current version December 3, 2012. This material is based upon work supported by the National Science Foundation under Grant CBET-1236370. Recommended for publication by Associate Editor B. Courtois upon evaluation of reviewers' comments.

The authors are with the Mechanical and Aerospace Engineering Department, University of Texas, Arlington, TX 76019 USA (e-mail: choobineh.leila@mavs.uta.edu; ankurjain@stanfordalumni.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCPMT.2012.2213820

rocal design symmetry, and so on [4]. 3-D IC technology may also enable modular design and manufacturing of system components such as memory. Due to the promising benefits of the 3-D IC technology, it is now an important component of the International Technology Roadmap for Semiconductors (ITRS) projections.

Much of the research focus in this field in the past decade or so has been on development of manufacturing technologies underlying 3-D ICs, such as etching and filling of deep vias, wafer thinning, and thin wafer handling, and so on [6], [7]. As these manufacturing technologies have become more and more mature, novel design methodologies are being investigated to take advantage of the unique features of the 3-D IC technology [3], [4]. Thermal-electrical co-design is particularly important in 3-D ICs due to the closely coupled nature of thermal and electrical performance. A number of papers have proposed design methodologies to recognize thermal constraints during the electrical design process of 3-D ICs [8]–[10]. Reconciliation of thermal and electrical design objectives during block-level floorplanning has been shown to significantly improve both thermal and electrical performances [8]. It has been shown that meeting a mixed electrical-thermal objective during floorplanning results in a configuration that does not expend significant thermal or electrical penalties [8]. On the other hand, a purely electrical optimization approach leads to a design for which thermal management is extremely challenging. Methodologies for exploiting reciprocal design symmetry for reducing peak temperature rise have also been proposed [4].

It is widely recognized that thermal management of 3-D ICs is a major technological barrier in widespread implementation of this technology [11], [12]. Stacking multiple silicon strata increases the power density without any enhancement in the footprint area available for heat removal. This problem is particularly exacerbated in the case of ultrathin wafers where the heat sources in adjacent die may be within 50 μ m of each other. The importance of thermal conduction through the micropad bonding layer between adjacent die has been characterized [11]. The role of TSVs for heat conduction away from local regions of high power densityoften referred to as hotspots—has been analyzed [13], [14]. While TSVs present several technological challenges in terms of mechanical stress development around the TSV, reliability, and so on [15], it has also been recognized that optimal placement of TSVs may aid in the thermal management of a 3-D IC.

A number of recent papers have investigated a variety of thermal management approaches for 3-D ICs. Liquid cooling of 3-D ICs has been evaluated [16]–[18]. Unfilled TSVs have been proposed to be used as conduits for supplying a cooling fluid to the interdie layers of 3-D ICs. Thermoelectric cooling of 3-D ICs has also been proposed [19]. While these novel approaches are quite promising, it is likely that they will be reserved only for very advanced applications such as high-performance computing. Thermal management of mainstream 3-D ICs will need to be done through smart electrical-thermal codesign that minimizes the thermal dissipation problem at its root and does not require expensive system-level thermal management.

The problem of increased power density in 3-D ICs was recognized quite early [20], [21], and a number of papers have investigated thermal management of 3-D ICs in the recent past [12]. Analytical, 1-D heat flow models have been developed [11]. While these models are a good first step toward understanding the thermal performance of 3-D ICs, they do not account for nonuniform heat generation, which is critical for accurate prediction of temperature fields in 3-D ICs. Some analytical models for heat conduction in multilayer structures have also been developed [22], [23]. These models do not fully capture the heat generation physics in 3-D ICs. For example, in the work by Geer et al. [22], power dissipation in a multilayer structure is modeled as volumetric heat generation which may not be an accurate model for 3-D ICs. Models based on nonvolumetric heat dissipation have also been proposed [23]. While these models are more comprehensive, heat generation only at one end of the multidie stack is accounted for, while interlayer heat generation is not considered. Numerical simulations have been conducted for predicting the temperature field in 3-D ICs [24]. While numerical simulations provide good results, they also suffer from several disadvantages. Usually, computational speed and interfacing with the electrical design flows are major concerns. Numerical models that are typically computed in a stand-alone software are difficult to interface with traditional electrical design and analysis codes. Numerical models for 3-D ICs also need to be validated against either experimental data or accurate analytical models. Development of analytical heat transfer models is thus highly desirable not only for reasons outlined above but also for developing a good basic understanding of the thermal management problem in 3-D ICs.

This paper develops analytical 3-D heat transfer models for 3-D ICs. Both steady-state and transient models are presented. These models are based on Fourier series expansion and Laplace transforms, respectively, and account for nonuniform heat generation at the device plane on each stratum in a multidie 3-D IC. Steady-state and transient temperature fields predicted by these models compare well with finite-element simulation results. These models present the temperature field in closed-form equations with minimal iteration requirements. Thus, these models are easier to integrate with other electrical design simulations as compared to finite-element analysis, which are typically carried out in a separate software package. In addition, analytical models enable parametric analysis of the heat transport problem and aid in novel thermal design



Fig. 1. Schematic of an N-die 3-D IC.

of 3-D ICs. Section II outlines the analytical model for determining the 3-D steady-state temperature field in a 3-D IC with nonuniform heat generation in each die. The model is used to solve for the die temperatures in two-die and three-die 3-D ICs for two different floorplans to illustrate the application of the model to a realistic problem. Section IV describes the transient model and discusses the results.

II. STEADY-STATE HEAT CONDUCTION MODEL FOR A 3-D IC

The geometry under consideration is shown in Fig. 1. The die stack consists of N die, each of size a by b. Thickness of the i^{th} die is c_i . The orientation of the x and y axes are common to each die. For brevity, x_i and y_i coordinates on each die are referred to as x and y, respectively. A heat sink is attached to the bottom-most die. Heat transfer from the bottom-most die to the air, which typically occurs through a thermal interface material, heat spreader, heat sink, and forced air cooling, is lumped together and modeled using a combined convective boundary condition, represented as h. For low-power applications where no heat sink is provided, the convective boundary condition models the heat dissipation through the electrical package. It is assumed that no heat loss occurs from the topmost die. All side surfaces are assumed to be adiabatic. Let $Q_i(x,y)$ be the heat generation in the device plane at the top of the i^{th} die. This analysis is greatly simplified by deriving the temperature field assuming that instead of all N heat sources, only the i^{*th} heat source $Q_{i^*}(x,y)$ the governing energy equations are linear, the temperature field due to each active heat layer may be computed separately and then added linearly to provide the temperature field due to all N heat sources.

Let $T_{i,i^*}(x,y,z_i)$ be the steady-state temperature rise in the *i*th die due to heat generation $Q_{i^*}(x,y)$ in the i^{*th} die. For brevity of nomenclature, the subscript i^* is omitted henceforth, and the temperature field in this case is represented as $T_i(x,y,z_i)$. Governing energy equations and boundary conditions are written and solved separately for each die. Let $q_i(x,y)$ be the heat flux entering the i^{th} die at $z_i = c_i$. Let k_i be the thermal conductivity of the i^{th} die. Let $T_{0i}(x,y)$ be the temperature profile at the intersecting plane between die *i* and i - 1. Assuming constant thermal conductivity, each $T_i(x,y,z_i)$ satisfies the following governing steady-state energy equation and adiabatic boundary conditions:

$$\frac{\partial^2 T_i}{\partial x^2} + \frac{\partial^2 T_i}{\partial y^2} + \frac{\partial^2 T_i}{\partial z_i^2} = 0$$
(1)

$$\frac{\partial T_i}{\partial x} = 0 \text{ at } x = 0, a \tag{2}$$

$$\frac{\partial T_i}{\partial y} = 0 \text{ at } y = 0, b.$$
(3)

The *z*-direction boundary conditions for $T_i(x,y,z_i)$ are given as follows:

For i = 1

$$\frac{\partial T_1}{\partial z_1} = \frac{h}{k_1} T_1 \text{ at } z_1 = 0 \tag{4}$$

$$\frac{\partial T_1}{\partial z_1} = \frac{1}{k_1} q_1(x, y) \text{ at } z_1 = c_1.$$
 (5)

For i = N

$$T_N = T_{0N}(x, y)$$
 at $z_N = 0$ (6)

$$\frac{\partial T_N}{\partial z_N} = 0 \text{ at } z_N = c_N. \tag{7}$$

For all other die

$$T_i = T_{0i}(x, y) \text{ at } z_i = 0$$
 (8)

$$\frac{\partial T_i}{\partial z_i} = u_i \cdot \frac{1}{k_i} q_i(x, y) \text{ at } z_i = c_i$$
(9)

where $u_i = \begin{vmatrix} 1 & i \leq i^* \\ -1 & i > i^* \end{vmatrix}$.

The term u_i accounts for the correct direction of heat flow below and above the heat source at the i^{*th} die.

The governing energy equations are solved by utilizing Fourier cosine series expansion [25]. Briefly, the temperature field is written as a two-variable infinite series comprising of products of the eigenfunctions in the x- and y-directions. An extra term is added in order to account for the zeroth term of the Fourier cosine expansion. This zeroth-order term is selected in such a way that it satisfies the respective z boundary condition. Finally, the coefficients of the infinite series are determined by comparing the coefficients with corresponding coefficients in the two-variable Fourier cosine series expansion of the nonhomogeneous boundary condition. The temperature fields are determined to be as follows.

For i = 1

$$T_1(x, y, z_1) = c_{1,0} \left(z_1 + \frac{k_1}{h} \right) + \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} c_{1,nm} \cos\left(\frac{n\pi x}{a}\right)$$
$$\times \cos\left(\frac{m\pi y}{b}\right) \left[\cosh\left(\gamma_{nm} z_1\right) + \frac{h}{k_1 \gamma_{nm}} \sinh\left(\gamma_{nm} z_1\right) \right] (10)$$

where $\gamma_{nm} = \sqrt{(n\pi/a)^2 + (m\pi/b)^2}$. For i = N

$$T_N(x, y, z_N) = c_{NB,0} + \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} c_{NB,nm} \cos\left(\frac{n\pi x}{a}\right) \\ \times \cos\left(\frac{m\pi y}{b}\right) \cosh\left(\gamma_{nm} \left(c_N - z_N\right)\right).$$
(11)

For $i \neq 1$ and $i \neq N$

$$T_{i}(x, y, z_{i}) = c_{iA,0}z_{i} + \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} c_{iA,nm} \cos\left(\frac{n\pi x}{a}\right) \cos\left(\frac{m\pi y}{b}\right)$$
$$\times \sinh\left(\gamma_{nm}z_{i}\right) + c_{iB,0} + \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} c_{iB,nm}$$
$$\times \cos\left(\frac{n\pi x}{a}\right) \cos\left(\frac{m\pi y}{b}\right) \cosh\left(\gamma_{nm}\left(c_{i}-z_{i}\right)\right).$$
(12)

Expressions for coefficients in (10)–(12) are given in the Appendix.

Note that the heat fluxes q_i and the intersecting temperatures T_{0i} are unknown, but they may be determined once temperature fields have been computed, using energy conservation and temperature continuity at the interface between adjacent die. It is thus possible to employ an iterative approach to solve for the temperature fields by initially guessing the heat fluxes q_i . The procedure is as follows.

- 1) Assume a value for the heat fluxes $q_i(x,y)$ for each die i = 1, 2, ..., N-1.
- 2) Solve for $T_1(x,y,z_1)$ from (10). Determine the interface temperature field between dies 1 and 2, $T_{02}(x,y) = T_1(x,y,z_1 = c_1)$.
- 3) Using T_{02} and the assumed value of q_2 , solve for $T_2(x,y,z_2)$ from (12). Determine $T_{03} = T_2(x,y,z_2 = c_2)$.
- 4) Repeat step 3 for each die from i = 2 to N 1, until $T_{N-1}(x,y,z_{N-1})$ is determined and is used to determine the interface temperature field $T_{0N}(x,y,z_N)$.
- 5) Determine $T_N(x,y,z_N)$ from (11).
- 6) Once all temperature fields have been computed, calculate the heat fluxes q_i

$$q_{i}(x, y) = \begin{vmatrix} u_{i}k_{i}\frac{\partial T_{i+1}}{\partial z_{i+1}} & i \neq i^{*} \\ Q_{i}^{*} - k_{i}\frac{\partial T_{i+1}}{\partial z_{i+1}} & i = i^{*}. \end{vmatrix}$$
(13)

7) Update the heat fluxes and repeat steps 1–6 until the change in the temperature fields between successive iterations is sufficiently small.

The analytical model is implemented by considering up to N_t terms in each double integral, which are evaluated using a 2-D Gauss quadrature [26]. Using this approach, the temperature field for a two-die stack and a three-die stack are computed and compared with finite-element-based simulations. For these simulations, each die is assumed to be 10×10 mm with 0.5-mm silicon thickness. For the two-die case, each die is assumed to have a hotspot dissipating 10 W over a 1×1 mm area centered at (2.5 mm, 2.5 mm) for die 1 and (7.5 mm, 7.5 mm) for die 2. The three-die case considers 10-W hotspots at (2.5 mm, 2.5 mm), (5.0 mm, 5.0 mm), and (7.5 mm, 7.5 mm) for dies 1–3, respectively. A convective heat transfer coefficient value, representative of typical forced air-cooling-based thermal management, is assumed for each case.

Fig. 2 shows a plot of N_t versus the temperature solution obtained at the center of the hotspot in die 1 in the three-die case. The resulting temperature is plotted as a fraction of the temperature if 1000 terms are used in the



Fig. 2. Plot showing the accuracy of the hotspot temperature computation as a function of the number of terms considered in (10), (13), and (16).



Fig. 3. Plot showing the temperature profile across the hotspot on die 1 as a function of the number of iterations carried out.

double summations in (10)–(12). Fig. 2 shows that around 25 terms are sufficient to reach within 1% of the temperature predicted by 1000 terms. This results in significant savings in computation time without sacrificing accuracy.

Fig. 3 shows a plot of the temperature curve along the *x*-direction at y = 2.5 mm for the device plane in die 1 for the three-die case at successive iterations. This plot shows that the temperature solution stabilizes within ± 0.5 °C within around seven iterations. Thus, a relatively small number of iterations are found to be sufficient for engineering accuracy.

Fig. 4(a) shows the temperature fields on dies 1 and 2 for the two-die case computed using the analytical model. Fig. 4(b) shows temperature curves along the x-direction at y = 2.5 mm and y = 7.5 mm for dies 1 and 2, respectively. Results are compared with finite-element simulation results which are carried out in a finite-element software package. Good agreement between the analytical model and finite-element



Fig. 4. (a) Computed temperature field for the two-die 3-D IC. (b) Cross-sectional temperature curve comparing the model with finite-element simulations.

simulation results is observed, with the maximum deviation between the two being around 4%. There is some waviness in the analytical solution as a result of representing the solution as a sum of cosine terms. This is observed to reduce as the number of terms in the solutions is increased.

Fig. 5(a) shows the temperature fields on dies 1–3 for the three-die case. Fig. 5(b) plots the temperature curves along the *x*-direction at y = 2.5 mm, y = 5.0 mm, and y = 7.5 mm for dies 1–3, respectively. Similar to the two-die case, comparison with finite-element simulation results shows excellent agreement, within 4% of each other. The deviation between the two is found to be further reduced by increasing the number of elements in the finite-element simulation or by employing finer domain discretization for calculating the double integrals for the analytical models. This shows the capability of the analytical model to compute temperature fields for 3-D ICs comprising more than two die. While the current research that this will lead to 3-D ICs with vertical integration of more than two die.

Section III illustrates the use of the steady-state analytical model to understand thermal optimization of the block-level floorplanning process [27]. It is shown that the analytical model may be used for temperature computation for blocklevel floorplans during the electrical design process of 3-D ICs. Significant reduction in steady-state temperature may be obtained by thermal-friendly placement of heat dissipating blocks in a multidie stack.



Fig. 5. (a) Computed temperature field for the three-die case. (b) Cross section of temperature profiles compared with finite-element simulations.

III. APPLICATION OF ANALYTICAL MODEL TO UNDERSTAND THERMAL-FRIENDLY FLOORPLANNING

A primary advantage of analytically derived expressions for the temperature distribution in a 3-D IC over finite-element simulations is the capability of being incorporated in the chip design flow with other electrical design considerations. This could be done, for example, by coding and compiling the temperature field equations derived in Section II in a higherlevel language such as C++. The resulting executables can be integrated much more easily with electronic design tools such as Verilog, SPICE, and so forth. Exchange of input and output parameters between the two could be utilized to make temperature computation an inherent part of each design iteration.

In this section, block-level floorplanning and 3-D IC temperature computation using the models presented in Section II is considered. This section considers a three-die stack for a four-core accelerated processing unit that integrates core



die3 die2 die1 Thermally Unfavorable Thermally Favorable Thermally Fa

(b)

Fig. 6. (a) Schematic showing the two floorplans considered. (b) Temperature plots on the device planes of the three die for the two floorplans.

computing and graphics processing capabilities. The models presented in this paper are used for rapid temperature field computation to aid thermal-friendly rearrangement of the floorplan, which results in significant reduction of peak temperature. The various blocks and their assumed power distributions are shown in Fig. 6(a). Blocks placed in the remaining space are assumed to dissipate small enough power density to be considered thermally insignificant. Two possible floorplans are considered. The first floorplan places cores in dies 2 and 3, and the graphics processing unit in die 1. The computed temperature field is shown in Fig. 6(b). It is clear that in this case, the close proximity of cores in dies 2 and 3 leads to a large local power density, and thus a large temperature rise. When the floorplan is redesigned to be more thermalfriendly by moving the cores to die 1-the die closest to the heat sink—and by avoiding spatial overlap between the cores, around 13% reduction in peak temperature is observed. While case (2) is not necessarily thermally optimal, it illustrates the process in which the models presented in this paper could be used for thermal design optimization of a 3-D IC. A general design optimization needs to consider not only thermal effects but also a variety of other factors, including electrical performance, manufacturability, and so on. By providing an analytical method for temperature computation, this paper contributes toward effective and optimal design of 3-D ICs.



Fig. 7. Schematic of the two-die stack for transient temperature field computation.

IV. TRANSIENT HEAT CONDUCTION MODEL FOR A 3-D IC

The transient governing energy equations for temperature fields in each die contain an extra transient term

$$\frac{\partial^2 T_i}{\partial x_i^2} + \frac{\partial^2 T_i}{\partial y_i^2} + \frac{\partial^2 T_i}{\partial z_i^2} = \frac{1}{\alpha_i} \frac{\partial T_i}{\partial t}$$
(14)

where α_i is the thermal diffusivity of the material of the *i*th stratum.

Spatial boundary conditions remain the same as in (2)–(9), except that the heat generation terms Q_i are now timedependent in general. It is assumed that the temperature field is zero at t = 0.

This transient heat conduction problem may be solved by combining the approach in Section II with Laplace transforms. Briefly, the Laplace transform is utilized to convert time-dependent PDE and boundary conditions for each $T_i(x, y, z_i, t)$ into time-independent PDE and boundary conditions in corresponding Laplacian fields $T_i(x, y, z_i)$. The resulting PDEs and boundary conditions are similar in nature to ones presented in Section II and are solved iteratively to determine $T_i(x, y, z_i)$. Inverse Laplace transforms are computed numerically to determine the time-dependent temperature fields $T_i(x, y, z_i, t)$ from the computed Laplacian fields $T_i(x, y, z_i)$. The de Hoog's quotient difference method algorithm [28] as implemented by Hollenbeck [29] is utilized for the numerical inversion. This procedure is illustrated using a two-die stack as follows.

Assume a two-die stack with nomenclature similar to the one presented in Section II. The two-die stack is shown in Fig. 7. Note that the orientation of the z_2 -axis is taken to be downward since this choice enables a more compact form of the solution. Heat sources $Q_1(x, y, t)$ and $Q_2(x, y, t)$ are assumed on the two die. Similar to the treatment in Section II, the temperature distributions $T_1(x, y, z_1, t)$ and $T_2(x, y, z_2, t)$ are split into contributions from $Q_1(x, y, t)$ alone and $Q_2(x, y, t)$ alone, and are superimposed for obtaining the final solution.

For the contributions from $Q_1(x, y, t)$ alone, the governing energy equations after applying Laplace transform for i = 1, 2are

$$\frac{\partial^2 \bar{T}_i}{\partial x^2} + \frac{\partial^2 \bar{T}_i}{\partial y^2} + \frac{\partial^2 \bar{T}_i}{\partial z_i^2} = \frac{p}{\alpha_i} \bar{T}_i$$
(15)

$$\frac{\partial \bar{T}_i}{\partial x} = 0 \text{ at } x = 0, a \tag{16}$$

$$\frac{\partial \bar{T}_i}{\partial y} = 0 \text{ at } y = 0, b \tag{17}$$

$$\frac{\partial T_1}{\partial z_1}\Big|_{z_1=0} = \frac{h}{k_1} \left. \bar{T}_1 \right|_{z_1=0} \qquad \frac{\partial T_2}{\partial z_2} \Big|_{z_2=0} = 0 \tag{18}$$

$$k_1 \left. \frac{\partial T_1}{\partial z_1} \right|_{z_1 = c_1} = \bar{q}_1(x_1, y_1) \qquad \bar{T}_2 \Big|_{z_2 = c_2} = \bar{T}_0(x_1, y_1) \quad (19)$$

where all variables with an overbar are Laplace transforms of corresponding variables, and p is the Laplace parameter.

The solutions for the Laplacian temperature fields are given by

$$\bar{T}_{i}(x, y, z_{i}) = c_{i0} \left(e^{\beta z_{i}} + A_{i} e^{-\beta z_{i}} \right) + \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} c_{i,nm} \cos\left(\frac{n\pi x}{a}\right) \cos\left(\frac{m\pi y}{b}\right) \times \left[\cosh\left(\gamma_{i,nm} z_{i}\right) + \frac{h_{i}}{k_{1} \gamma_{i,nm}} \sinh\left(\gamma_{i,nm} z_{i}\right) \right]$$
(20)

where $\beta_i = \sqrt{p/\alpha_i}$, $\gamma_{i,nm} = \sqrt{(n\pi/a)^2 + (m\pi/b)^2 + \beta_i^2}$ and $A_i = (\beta_i - (h_i/k_i))/(\beta_i + (h_i/k_i))$ for i = 1, 2.

Expressions for $c_{i,0}$ and $c_{i,nm}$ for i = 1, 2 are given in the Appendix.

Due to the respective boundary conditions at the heat sink and package ends, $h_1 = h$ and $h_2 = 0$ in (20). Note that the intermediate temperature $T_0(x,y)$ and heat flux $q_1(x,y)$ are not known in advance. However, the solution may be determined iteratively using a procedure similar to the one outlined in Section II.

For the contributions from $Q_2(x, y, z_2, t)$ alone, the governing energy equations after applying the Laplace transform for i = 1, 2 are

$$\frac{\partial^2 \bar{T}_i}{\partial x^2} + \frac{\partial^2 \bar{T}_i}{\partial y^2} + \frac{\partial^2 \bar{T}_i}{\partial z_i^2} = \frac{p}{\alpha_i} \bar{T}_i \qquad (21)$$

$$\frac{\partial \bar{T}_i}{\partial x} = 0 \text{ at } x = 0, a \qquad (22)$$

$$\frac{\partial T_i}{\partial y} = 0 \text{ at } y = 0, b \tag{23}$$

$$\frac{\partial \bar{T}_1}{\partial z_1}\Big|_{z_1=0} = \frac{h}{k_1} \left. \bar{T}_1 \right|_{z_1=0} \qquad \frac{\partial \bar{T}_2}{\partial z_2} \Big|_{z_2=0} = \bar{Q}_2(x, y) \quad (24)$$

$$k_1 \left. \frac{\partial T_1}{\partial z_1} \right|_{z_1 = c_1} = \bar{q}_1(x, y) \qquad \bar{T}_2 \Big|_{z_2 = c_2} = \bar{T}_0(x, y). \tag{25}$$

The solution for $\overline{T}_1(x, y, z_1)$ is the same as given in (20). The solution for $\overline{T}_2(x, y, z_2)$ is given by

$$\bar{T}_{2}(x, y, z_{2}) = c_{2A,0} \left(e^{\beta_{2}(z_{2}-c_{2})} - e^{-\beta_{2}(z_{2}-c_{2})} \right) + \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} c_{2A,nm}$$

$$\times \cos \left(\frac{n\pi x}{a} \right) \cos \left(\frac{m\pi y}{b} \right) \sinh \left(\gamma_{nm} \left(z_{2} - c_{2} \right) \right)$$

$$+ c_{2B,0} \left(e^{\beta_{2}z_{2}} + e^{-\beta_{2}z_{2}} \right) + \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} c_{2B,nm}$$

$$\times \cos \left(\frac{n\pi x}{a} \right) \cos \left(\frac{m\pi y}{b} \right) \cosh \left(\gamma_{nm} z_{2} \right). \quad (26)$$



Fig. 8. Comparison of transient temperature profile at the hotspot in a two-die 3-D IC predicted by the analytical model and finite-element simulations.

Expressions for $c_{2A,0}$, $c_{2B,0}$, $c_{2A,nm}$, and $c_{2B,nm}$ are given in the Appendix.

Once the solutions for the Laplace transforms of the temperature fields for heat generation on each die have been determined, the actual temperature field is determined by numerically evaluating the inverse Laplace transform.

Fig. 8 shows the temperature as a function of time at the hotspot on die 1 for the two-die case described above. Excellent agreement within 2.6% of finite element simulation results is observed. The model presented in this section may be helpful in characterizing the transient thermal behavior of 3-D ICs during events of core startup or shutdown, core switching, and so forth, where there is significant transient behavior of power sources.

V. CONCLUSION

This paper presented an analytical model to determine 3-D steady-state and transient temperature fields in a 3-D IC, based on the solutions of the governing energy equations. An iterative approach that takes advantage of temperature and energy conservation at interfaces was proposed. The temperature solution based on this approach converges within around seven iterations, and is in good agreement with finite-element simulation results. The analytical approach provides good physical insight into the problem of determining temperature fields in 3-D ICs. In addition, it is expected to more easily interface with mainstream electrical design tools as compared to finite-element-based methods. This paper also underscores the need for thermal-friendly pre-silicon design, which helps minimize the system-level thermal dissipation challenge and leads to higher reliability without compromising electrical performance. This paper is expected to aid in developing temperature characterization and prediction tools for 3-D ICs. In addition, this paper may also help in the characterization of various thermal management strategies being proposed for 3-D ICs.

APPENDIX

The coefficients $c_{1,0}$ and $c_{1,nm}$ for (10) are given by

$$c_{1,0} = \frac{1}{abk_1} \int_{y=0}^{b} \int_{x=0}^{a} q_1(x, y) dx dy$$
(27)
$$c_{1,nm} = \begin{vmatrix} \frac{2}{abk_1 P_{nm}} \int_{y=0}^{b} \int_{x=0}^{a} q_1(x, y) \cos\left(\frac{n\pi x}{a}\right) dx dy \\ n \neq 0; m = 0 \\ \frac{2}{abk_1 P_{nm}} \int_{y=0}^{b} \int_{x=0}^{a} q_1(x, y) \cos\left(\frac{m\pi y}{b}\right) dx dy \\ n = 0; m \neq 0 \\ \frac{4}{abk_1 P_{nm}} \int_{y=0}^{b} \int_{x=0}^{a} q_1(x, y) \cos\left(\frac{n\pi x}{a}\right) \\ \times \cos\left(\frac{m\pi y}{b}\right) dx dy \quad n \neq 0; m \neq 0$$
(28)

where $P_{nm} = \gamma_{nm} \sinh(\gamma_{nm}c_1) + (h/k_1) \cosh(\gamma_{nm}c_1)$.

The coefficients $c_{Nb,0}$ and $c_{Nb,nm}$ for (11) are given by

$$c_{Nb,0} = \frac{1}{ab} \int_{y=0}^{b} \int_{x=0}^{a} T_{0N}(x, y) dx dy$$
(29)
$$c_{Nbnm} = \begin{vmatrix} \frac{2}{ab \cosh(y_{nm}c_N)} \int_{y=0}^{b} \int_{x=0}^{a} T_{0N}(x, y) \\ \times \cos\left(\frac{n\pi x}{a}\right) dx dy & n \neq 0; m = 0 \\ \frac{2}{ab \cosh(y_{nm}c_N)} \int_{y=0}^{b} \int_{x=0}^{a} T_{0N}(x, y) \\ \times \cos\left(\frac{m\pi y}{b}\right) dx dy & n = 0; m \neq 0 \\ \frac{4}{ab \cosh(y_{nm}c_N)} \int_{y=0}^{b} \int_{x=0}^{a} T_{0N}(x, y) \\ \times \cos\left(\frac{n\pi x}{a}\right) \cos\left(\frac{m\pi y}{b}\right) dx dy & n \neq 0; m \neq 0. \end{cases}$$
(30)

The coefficients $c_{iA,0}$ and $c_{iA,nm}$ for (12) are given by

$$c_{iA,0} = \frac{1}{abk_{i}} \int_{y=0}^{b} \int_{x=0}^{a} u_{i} \cdot q_{i}(x, y) dx dy$$
(31)
$$c_{iA,nm} = \begin{vmatrix} \frac{2u_{i}}{abk_{i}\gamma_{nm}\cosh(\gamma_{nm}c_{i})} \int_{y=0}^{b} \int_{x=0}^{a} q_{i}(x, y) \cos\left(\frac{n\pi x}{a}\right) dx dy \\ n \neq 0; m = 0 \\ \frac{2u_{i}}{abk_{i}\gamma_{nm}\cosh(\gamma_{nm}c_{i})} \int_{y=0}^{b} \int_{x=0}^{a} q_{i}(x, y) \cos\left(\frac{m\pi y}{b}\right) dx dy \\ n = 0; m \neq 0 \\ \frac{4u_{i}}{abk_{i}\gamma_{nm}\cosh(\gamma_{nm}c_{i})} \int_{y=0}^{b} \int_{x=0}^{a} q_{i}(x, y) \cos\left(\frac{n\pi x}{a}\right) \\ \times \cos\left(\frac{m\pi y}{b}\right) dx dy \quad n \neq 0; m \neq 0.$$
(32)

The coefficients $c_{iB,0}$ and $c_{iB,nm}$ for (12) are given by

$$c_{iB,0} = \frac{1}{ab} \int_{y=0}^{b} \int_{x=0}^{a} T_{0i}(x, y) dx dy$$
(33)
$$c_{iB,nm} = \begin{vmatrix} \frac{2}{ab \cosh(y_{nm}c_i)} \int_{y=0}^{b} \int_{x=0}^{a} T_{0i}(x, y) \cos\left(\frac{n\pi x}{a}\right) dx dy \\ n \neq 0; m = 0 \\ \frac{2}{ab \cosh(y_{nm}c_i)} \int_{y=0}^{b} \int_{x=0}^{a} T_{0i}(x, y) \cos\left(\frac{m\pi y}{b}\right) dx dy \\ n = 0; m \neq 0 \\ \frac{4}{ab \cosh(y_{nm}c_i)} \int_{y=0}^{b} \int_{x=0}^{a} T_{0i}(x, y) \cos\left(\frac{n\pi x}{a}\right) \\ \times \cos\left(\frac{m\pi y}{b}\right) dx dy \quad n \neq 0; m \neq 0.$$
(34)

The coefficients $c_{1,0}$ and $c_{1,nm}$ for (20) are given by

$$c_{1,0} = \frac{1}{abk_1\beta_1 \left(e^{\beta_1c_1} - A_1e^{-\beta_1c_1}\right)} \int_{y=0}^{b} \int_{x=0}^{a} \bar{q}_1(x, y) dx dy$$
(35)
$$c_{1nm} = \begin{vmatrix} \frac{2}{abk_1P_{1,nm}} \int_{y=0}^{b} \int_{x=0}^{a} \bar{q}_1(x, y) \cos\left(\frac{n\pi x}{a}\right) dx dy \\ n \neq 0; m = 0 \\ \frac{2}{abk_1P_{1,nm}} \int_{y=0}^{b} \int_{x=0}^{a} \bar{q}_1(x, y) \cos\left(\frac{m\pi y}{b}\right) dx dy \\ n = 0; m \neq 0 \\ \frac{4}{abk_1P_{1,nm}} \int_{y=0}^{b} \int_{x=0}^{a} \bar{q}_1(x, y) \cos\left(\frac{n\pi x}{a}\right) \\ \times \cos\left(\frac{m\pi y}{b}\right) dx dy \quad n \neq 0; m \neq 0$$
(36)

where $P_{1,nm} = \gamma_{1,nm} \sinh (\gamma_{1,nm}c_1) + (h/k_1) \cosh (\gamma_{1,nm}c_1)$. The coefficients $c_{2,0}$ and $c_{2,nm}$ for (20) are given by

$$c_{2,0} = \frac{1}{ab \left(e^{\beta_2 c_2} + A_2 e^{-\beta_2 c_2}\right)} \int_{y=0}^{b} \int_{x=0}^{a} \bar{T}_0(x, y) dx dy \quad (37)$$

$$c_{2,nm} = \begin{vmatrix} \frac{2}{ab P_{2,nm}} \int_{y=0}^{b} \int_{x=0}^{a} \bar{T}_0(x, y) \cos\left(\frac{n\pi x}{a}\right) dx dy \\ n \neq 0; m = 0 \\ \frac{2}{ab P_{2,nm}} \int_{y=0}^{b} \int_{x=0}^{a} \bar{T}_0(x, y) \cos\left(\frac{m\pi y}{b}\right) dx dy \\ n = 0; m \neq 0 \\ \frac{4}{ab P_{2,nm}} \int_{y=0}^{b} \int_{x=0}^{a} \bar{T}_0(x, y) \cos\left(\frac{n\pi x}{a}\right) \\ \times \cos\left(\frac{m\pi y}{b}\right) dx dy \quad n \neq 0; m \neq 0$$

$$(38)$$

where $P_{2,nm} = \cosh(\gamma_{2,nm}c_2) + (h/k_2\gamma_{2,nm})\sinh(\gamma_{2,nm}c_2)$.

The coefficients $c_{2A,0}$, $c_{2B,0}$, $c_{2A,nm}$, and $c_{2B,nm}$ for (26) are given by

$$c_{2A,0} = \frac{1}{abk_2\beta_2 \left(e^{\beta_2 c_2} + e^{-\beta_2 c_2}\right)} \int_{y=0}^{b} \int_{x=0}^{a} -\bar{Q}_2(x, y) dx dy$$
(39)

$$c_{2B,0} = \frac{1}{ab\left(e^{\beta_2 c_2} + e^{-\beta_2 c_2}\right)} \int_{y=0}^{b} \int_{x=0}^{a} \bar{T}_0(x, y) dx dy \qquad (40)$$

$$c_{2A,nm} = \begin{vmatrix} \frac{2}{abk_2\gamma_{2,nm}\cosh(\gamma_{2,nm}c_2)} \int\limits_{y=0}^{b} \int\limits_{x=0}^{a} -\bar{Q}_2(x, y) \\ \times \cos\left(\frac{n\pi x}{a}\right) dx dy & n \neq 0; m = 0 \\ \frac{2}{abk_2\gamma_{2,nm}\cosh(\gamma_{2,nm}c_2)} \int\limits_{y=0}^{b} \int\limits_{x=0}^{a} -\bar{Q}_2(x, y) \\ \times \cos\left(\frac{m\pi y}{b}\right) dx dy & n = 0; m \neq 0 \\ \frac{4}{abk_2\gamma_{2,nm}\cosh(\gamma_{2,nm}c_2)} \int\limits_{y=0}^{b} \int\limits_{x=0}^{a} -\bar{Q}_2(x, y) \cos\left(\frac{n\pi x}{a}\right) \\ \times \cos\left(\frac{m\pi y}{b}\right) dx dy & n \neq 0; m \neq 0 \end{cases}$$
(41)

$$c_{2B,nm} = \begin{vmatrix} \frac{2}{ab \cosh(y_{2,nm}c_2)} \int_{y=0}^{b} \int_{x=0}^{a} \bar{T}_0(x, y) \cos\left(\frac{n\pi x}{a}\right) dx dy \\ & n \neq 0; m = 0 \\ \frac{2}{ab \cosh(y_{2,nm}c_2)} \int_{y=0}^{b} \int_{x=0}^{a} \bar{T}_0(x, y) \cos\left(\frac{m\pi y}{b}\right) dx dy \\ & n = 0; m \neq 0 \\ \frac{4}{ab \cosh(y_{2,nm}c_2)} \int_{y=0}^{b} \int_{x=0}^{a} \bar{T}_0(x, y) \cos\left(\frac{n\pi x}{a}\right) \\ & \times \cos\left(\frac{m\pi y}{b}\right) dx dy \quad n \neq 0; m \neq 0 \end{cases}$$
(42)

$$c_{2,nm} = \begin{cases} \frac{2}{abP_{2,nm}} \int\limits_{y=0}^{b} \int\limits_{x=0}^{a} \bar{T}_{0}(x, y) \cos\left(\frac{n\pi x}{a}\right) dx dy \\ n \neq 0; m = 0 \\ \frac{2}{abP_{2,nm}} \int\limits_{y=0}^{b} \int\limits_{x=0}^{a} \bar{T}_{0}(x, y) \cos\left(\frac{m\pi y}{b}\right) dx dy \\ n = 0; m \neq 0 \\ \frac{4}{abP_{2,nm}} \int\limits_{y=0}^{b} \int\limits_{x=0}^{a} \bar{T}_{0}(x, y) \cos\left(\frac{n\pi x}{a}\right) \\ \times \cos\left(\frac{m\pi y}{b}\right) dx dy \quad n \neq 0; m \neq 0 \end{cases}$$
(43)

where $P_{2,nm} = \cosh(\gamma_{2,nm}c_2) + (h/k_2\gamma_{2,nm})\sinh(\gamma_{2,nm}c_2)$.

REFERENCES

- K. Banerjee, S. J. Souri, and K. C. Saraswat, "3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proc. IEEE*, vol. 89, no. 5, pp. 602–633, May 2001.
- [2] R. Patti, "Three-dimensional integrated circuits and the future of systemon-chip designs," *Proc. IEEE*, vol. 94, no. 6, pp. 1214–1224, Jun. 2006.
- [3] G. Loh, Y. Xie, and B. Black, "Processor design in 3D die-stacking technologies," *IEEE Micro*, vol. 27, no. 3, pp. 31–48, May–Jun. 2007.
- [4] S. M. Alam, R. E. Jones, S. Pozder, R. Chatterjee, and A. Jain, "Interstratum connection design considerations for cost-effective 3-D system integration," *IEEE Trans Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 3, pp. 450–460, Mar. 2010.

- [5] I. Savidis, S. Alam, A. Jain, S. Pozder, R. E. Jones, and R. Chatterjee, [22] J. Geer, A
- "Electrical modeling and characterization of through-silicon vias (TSVs) for 3-D integrated circuits," *Microelectron. J.*, vol. 41, no. 1, pp. 9–16, 2010.
 [6] S. Porder, P. Chatterico, A. Jain, Z. Hueng, P. F. Jones, and F. Acosta.
- [6] S. Pozder, R. Chatterjee, A. Jain, Z. Huang, R. E. Jones, and E. Acosta, "Progress of 3D integration technologies and 3D interconnects," in *Proc. IEEE Int. Interconnect Technol. Conf.*, San Francisco, CA, Jul. 2007, pp. 213–215.
- [7] P. R. Morrow, C.-M. Park, S. Ramanathan, M. J. Kobrinsky, and M. Harmes, "Three-dimensional wafer stacking via Cu–Cu bonding integrated with 65-nm strained-Si/low-k CMOS technology," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 335–337, May 2006.
- [8] A. Jain, S. M. Alam, S. Pozder, and R. E. Jones, "Thermal-electrical co-optimisation of floorplanning of three-dimensional integrated circuits under manufacturing and physical design constraints," *IET Comput. Digital Tech.*, vol. 5, no. 3, pp. 169–178, May 2011.
- [9] B. Goplen and S. Sapatnekar, "Efficient thermal placement of standard cells in 3D ICs using a force directed approach," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design*, Nov. 2003, pp. 86–89.
- [10] J. Cong, J. Wei, and Y. Zhang, "A thermal-driven floorplanning algorithm for 3D ICs," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design*, Nov. 2004, pp. 306–313.
- [11] A. Jain, R. E. Jones, R. Chatterjee, S. Pozder, and Z. Huang, "Analytical and numerical modeling of the thermal performance of threedimensional integrated circuits," *IEEE Trans. Comp. Packag. Technol.*, vol. 33, no. 1, pp. 56–63, Mar. 2010.
- [12] V. Venkatadri, B. Sammakia, K. Srihari, and D. Santos, "A review of recent advances in thermal management in three dimensional chip stacks in electronic systems," *ASME J. Electron. Packag.*, vol. 133, no. 4, pp. 041011-1–041011-15, 2011.
- [13] J. Cong, G. Luo, J. Wei, and Y. Zhang, "Thermal-aware 3D IC placement via transformation," in *Proc. Asia South Pacific Design Autom. Conf.*, 2007, pp. 780–785.
- [14] B. Goplen and S. S. Sapatnekar, "Placement of thermal vias in 3-D ICs using various thermal objectives," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 26, no. 4, pp. 692–709, Apr. 2006.
- [15] K. H. Lu, X. Zhang, S.-K. Ryu, J. Im, R. Huang, and P. S. Ho, "Thermomechanical reliability of 3-D ICs containing through silicon vias," in *Proc. Electron. Comp. Technol. Conf.*, 2009, pp. 630–634.
- [16] C. R. King, J. Zaveri, M. S. Bakir, and J. D. Meindl, "Electrical and fluidic C4 interconnections for inter-layer liquid cooling of 3D ICs," in *Proc. Electron. Comp. Technol. Conf.*, 2010, pp. 1674–1681.
- [17] Y. J. Kim, Y. K. Joshi, A. G. Federov, Y. J. Lee, and S. K. Lim, "Thermal characterization of interlayer microfluidic cooling of three-dimensional integrated circuits with nonuniform heat flux," *ASME J. Heat Transfer*, vol. 132, no. 4, p. 041009, 2010.
- [18] T. Brunschwiler, B. Michel, H. Rothuizen, U. Kloter, B. Wunderle, H. Oppermann, and H. Reichl, "Interlayer cooling potential in vertically integrated packages," *Microsyst. Technol.*, vol. 15, no. 1, pp. 57–74, 2009.
- [19] H. N. Phan and D. Agonafer, "Experimental analysis model of an active cooling method for 3D-ICs utilizing a multidimensional configured thermoelectric," in *Proc. IEEE SEMI-THERM Symp.*, Feb. 2010, pp. 55–58.
- [20] M. B. Kleiner, S. A. Kuhn, P. Ramm, and W. Weber, "Thermal analysis of vertically integrated circuits," in *IEDM Tech. Dig.*, 1995, pp. 487–490.
- [21] T.-Y. Chiang, S. J. Souri, C. O. Chui, and K. C. Saraswat, "Thermal analysis of heterogeneous 3-D ICs with various integration scenarios," in *IEDM Tech. Dig.*, 2001, pp. 681–684.

- [22] J. Geer, A. Desai, and B. Sammakia, "Heat conduction in multilayered rectangular domains," *ASME J. Electron. Packag.*, vol. 129, no. 4, pp. 440–451, 2007.
- [23] A. Haji-Sheikh, J. V. Beck, and D. Agonafer, "Steady-state heat conduction in multilayer bodies," *Int. J. Heat Mass Transfer*, vol. 46, no. 13, pp. 2363–2379, 2003.
- [24] K. Puttaswamy and G. H. Loh, "Thermal analysis of a 3D die-stacked high-performance microprocessor," in *Proc. ACM/IEEE Great Lakes Symp. VLSI*, May 2006, pp. 19–24.
- [25] H. S. Carslaw and J. C. Jaeger, Conduction of Heat in Solids, 2nd ed. New York: Oxford Univ. Press, 1986.
- [26] R. W. Hamming, Numerical Methods for Scientists and Engineers, 2nd ed. New York: Dover, 1986.
- [27] M. Sarrafzadeh and C. K. Wong, An Introduction to VLSI Design, 1st ed. New York: McGraw-Hill, 1996.
- [28] F. R. de Hoog, J. H. Knight, and A. N. Stokes, "An improved method for numerical inversion of Laplace transforms," *SIAM. J. Sci. Stat. Comput.*, vol. 3, no. 3, pp. 357–366, 1982.
- [29] K. J. Hollenbeck. (1998). INVLAP.M: A MATLAB Function for Numerical Inversion of Laplace Transforms by the de Hoog Algorithm [Online]. Available: http://www.isva.dtu.dk/staff/karl/invlap.htm



Leila Choobineh received the B.S. degree from Shiraz University, Shiraz, Iran, and the M.S. degree from Shahrekord University, Shahrekord, Iran, both in mechanical engineering. She is currently pursuing the Doctoral degree with the Department of Mechanical and Aerospace Engineering, University of Texas at Arlington, Arlington.

Her research interests include thermal modeling of 3-D integrated circuits and microfabrication.



Ankur Jain received the B.Tech. degree from the Indian Institute of Technology, Delhi, India, in 2001, and the M.S. and Ph.D. degrees from Stanford University, Stanford, CA, in 2003 and 2007, respectively, all in mechanical engineering.

He is an Assistant Professor with the Department of Mechanical and Aerospace Engineering, University of Texas at Arlington, Arlington. He held various research and development positions in the semiconductor industry from 2007 to 2011. He has delivered invited talks and tutorials in his

areas of expertise at numerous international conferences and workshops. His research interests include microscale thermal transport, thermal management of microelectronics, bioheat transfer, microelectromechanical systems, and nanomanufacturing.