

Determination of temperature distribution in three-dimensional integrated circuits (3D ICs) with unequally-sized die



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HIGHLIGHTS

- A model is developed for the three-dimensional temperature field in unequally-sized 3D integrated circuits.
- Model results are in excellent agreement with finite-element simulation models.
- Model enables a fundamental understanding of thermal management challenges in 3D ICs.
- An unequally-sized 3D IC has higher temperature rise than equivalent uniform 3D IC due to thermal constriction/spreading.

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ABSTRACT

There is much interest in 3D integrated circuits (3D IC) technology for vertical integration of multiple device planes in semiconductor devices. Stacking several device planes vertically offers significant electrical performance improvements. This can also lead to reduced design and manufacturing costs. Several 3D IC manufacturing and packaging approaches require adjacent die sizes to be different from one another since this facilitates differentiated manufacturing and design. However, it is expected that unequally-sized die may cause deteriorated thermal performance due to heat spreading and constriction. This manuscript presents a heat transfer model for predicting the three-dimensional temperature field in a multi-die 3D IC with unequally-sized die. This problem is solved iteratively using solutions of three simpler heat transfer problems outlined in the manuscript. Temperature fields predicted by the model are in close agreement with finite-element simulation results. The model is used to compare the thermal performance of unequally-sized die stacks with a uniformly-sized die stack. Results indicate that the greater the degree of non-uniformity in the die stack, the greater is the peak temperature rise. The model and results presented in this manuscript are expected to aid in the development of effective thermal design tools for 3D ICs.

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1. Introduction

Three-dimensional integrated circuits (3D IC) technology refers to the vertical integration of circuits on multiple semiconductor substrates [1,2]. 3D ICs offer several advantages over traditional microelectronic designs, including heterogenous design integration, reduced interconnect delay, etc. [3,4]. It has been estimated that 3D integration provides roughly the same performance benefits as dimensional scaling by one technology node without the prohibitive associated costs [5–7]. Vertical integration is usually implemented by bonding of metal pads on frontside or backside of adjacent die, which in addition to mechanical adhesion also

provide a pathway for electrical communication between the die [3]. 3D IC technology also often necessitates signal transmission from one face of a die to the other. This is usually implemented using through-silicon vias (TSVs), which are metal-filled vias etched all the way through the substrate [7].

Thermal management of 3D ICs has been widely recognized as a significant technology challenge for widespread implementation of this technology [6,8–10]. Like traditional microelectronic chips, temperature rise and temperature uniformity is a concern in 3D ICs, since temperature and thermomechanical stresses generated due to temperature differential both adversely affect transistor performance. Thermomechanical stresses also adversely affect chip–package interactions and reliability. While the back face of the die was traditionally available for heat removal, for example by attachment to a heat sink using a thermal interface material, both faces of the die on a 3D IC are utilized for electrical interconnection

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Nomenclature

Symbols

a, b, c	die dimensions
d	coefficient
h	Heat transfer coefficient ($\text{Wm}^{-2}\text{K}^{-1}$)
k	thermal conductivity ($\text{Wm}^{-1}\text{K}^{-1}$)
n, m	indices for infinite series solutions for temperature rise
p	coefficient
Q	heat flux (Wm^{-2})
T	temperature rise (K)
x, y, z	spatial coordinates (m)

Subscript

g	guessed temperature field
i	Die number

with adjacent die. The heat removal challenge is particularly exacerbated for die in the middle of the vertical stack. Early work in this field focused on investigation of thermal management challenges in 3D ICs [11,12] and the thermal implications of various electrical design models being considered for 3D IC technology [13,14].

Thermal envelope available for 3D IC design has been estimated by modeling changes in block-level power consumption due to three-dimensional design and its impact on thermal management [15]. A number of thermal management approaches have been investigated for meeting the heat dissipation challenge in 3D ICs [16–20]. These approaches include liquid cooling [16–19], thermoelectrics-based cooling [20], etc. A limited amount of experimental work on measurement of thermal characteristics of 3D ICs has also been reported in the past few years [21–24]. Recent work has reported the use of a novel thermal lid for thermal management of unequally sized die stack [36].

While most of the thermal modeling work for 3D ICs has assumed identically sized die [9,25–28], manufacturing and packaging considerations often require that the die size not be the same [6]. For example, making the bottom die larger than the top die allows wire bond connections to be made to the exposed area of the bottom die. Further, by employing die-on-wafer bonding, significant yield improvement can be obtained without requiring the die to be the same size [6]. Finally, having unequally sized die is also necessitated by implementation of heterogeneous design. For example, the same memory die designed using a pre-specified bond pad layout could be implemented on multiple logic die designs for different applications, none of which need to necessarily be the same size [4]. The memory die does not need to be designed for each application separately, resulting in significant reduction in cost and design time.

The nature of heat transfer in unequally-sized die is inherently different from a stack of identical die due to heat spreading and constriction. A variety of thermal simulation approaches including finite-difference and finite-element modeling have been employed for determining the temperature field in a 3D IC [26,27,29,30]. Analytical heat transfer models developed for uniformly-sized die [31–33] are not applicable if the die sizes are not uniform. Edge effects, which are usually neglected in the analysis of identical die may be important for unequally-sized die. Past work on heat spreading and constriction in electronic packages has only considered two layers of unequally-sized substrates [34]. Another paper reported finite-difference modeling of heat conduction in unequally-sized 3D

IC stacks [35]. While such approaches help determine the temperature profile in a 3D IC, a more fundamental approach involving analytical solutions of the governing energy equations would help develop a basic understanding of thermal management of unequally-sized 3D IC stacks, and how such stacks differ from uniformly-sized stacks. Given the growing interest in thermal management of 3D ICs in general, and unequally-sized die stacks in particular, it is essential to develop a fundamental understanding of this problem and derive analytical expressions for the temperature field based on solutions of the governing energy equations. Such approach is likely to help improve thermal design of 3D ICs.

This paper presents an analytical model for understanding heat transfer characteristics of a stack of unequally sized die with non-uniform heating on each die. Governing energy conservation equations with appropriate boundary conditions are solved, resulting in three-dimensional temperature fields for each die. The non-uniform die size presents interesting modeling challenges, necessitating an iterative approach for determining the temperature field. Results are in close agreement with finite-element simulations. The model is used for comparing the thermal performance of non-uniform 3D ICs with a uniformly-sized 3D IC. It is found that the larger the degree of non-uniformity in die size, the higher is the temperature, due to additional thermal spreading/constriction resistance. This work provides a useful tool for understanding the fundamentals of heat transfer in 3D ICs and evaluating the realistic thermal impact of 3D integration.

2. Steady-state heat conduction model for non-uniformly sized 3D IC

The die stack consists of N dies, each of which is a cuboid of size a_i by b_i by c_i . Fig. 1 shows the x - z cross-section of the geometry under consideration. All dies in the stack are assumed to be centered around a common axis. The model presented in this manuscript can also be used for non-concentric die stacks with appropriate transformations in the x and y axes. A heat sink is attached to the bottom-most die, which is modeled using a convective boundary condition. It is assumed that the top-most die is connected to the electrical package, heat loss through which is neglected. This is a reasonable assumption because of the presence of the mother board and other electrical units on the package end

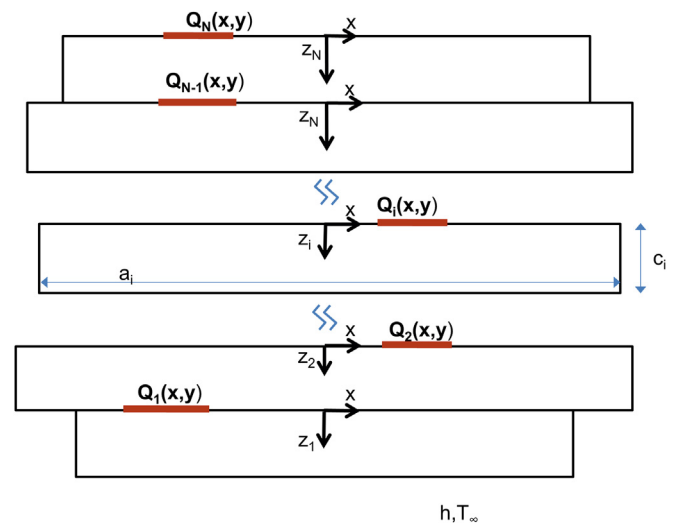


Fig. 1. Schematic of the cross-section view of the N -die stack comprising unequally sized die. The size of the i th die in the direction perpendicular to the paper is b_i . All die are assumed to be concentric, and the origin of coordinates for each die is assumed to be located at the center of the top x - y plane of the die.

that inhibit heat flow through that route. Typical thermal resistance of the package is much higher than the heat sink, resulting in most heat flowing through the heat sink. All side surfaces are assumed to be adiabatic. $Q_i(x,y)$ is the known heat generation that occurs in the device plane at the top of the i th die. The primary interest is in determining the temperature fields $T_i(x,y,z_i)$.

The model for determining temperature in the N-die stack requires solutions for three heat transfer problems pertaining to a single die. These problems and their solutions are presented in Section 2.1. Section 2.2 combines these solutions to provide a model for the N-die temperature field.

2.1. Solution to three relevant heat transfer problems

Fig. 2 schematically shows three heat transfer problems in a single die that are relevant for the problem being considered in this paper. The multi-die problem will be split into several sub-problems, each of which will be shown to be equivalent to one of the three problems shown in Fig. 2. Each problem shown in Fig. 2 comprises a single die of size a by b by c , with a temperature-independent thermal conductivity k . In each problem, a heat flux $q(x,y)$ is incident on the top surface of the die, and the side walls are adiabatic. Problems 1–3 differ in the boundary condition at the bottom face. In problem 1, heat loss occurs through the bottom, which is modeled using a convective heat transfer coefficient h . In problem 2, the temperature profile $T_0(x,y)$ is known on the bottom face. In problem 3, the temperature is known to be $T_0(x,y)$ in a region bound by $a_1 \leq x \leq a_2$ and $b_1 \leq y \leq b_2$, whereas the remainder of the bottom face is adiabatic.

For problem 1, the governing equation for steady state temperature rise $T(x,y,z)$ is

$$\frac{\partial T}{\partial z} = -\frac{1}{k}q(x,y) \quad \text{at } z = 0 \tag{4}$$

$$\frac{\partial T}{\partial z} = -\frac{h}{k}T \quad \text{at } z = c \tag{5}$$

Problem 1 is solved by utilizing Fourier cosine series expansion [37]. Briefly, the temperature field is written as a two-variable infinite series comprising products of the eigenfunctions in x and y directions. The coefficients of the infinite series are determined by using the non-homogenous boundary condition and comparing the coefficients with corresponding coefficients in the two-variable Fourier cosine series expansion of the non-homogenous term. The solution for the temperature field $T(x,y,z)$ is as follows:

$$T(x,y,z) = d_0 \left((c-z) + \frac{k}{h} \right) + \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} d_{nm} \cos\left(\frac{n\pi(x-0.5a)}{a}\right) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) \times \left[\cosh(\gamma_{nm}(c-z)) + \frac{h}{k\gamma_{nm}} \sinh(\gamma_{nm}(c-z)) \right] \tag{6}$$

where $\gamma_{nm} = \sqrt{\left(\frac{n\pi}{a}\right)^2 + \left(\frac{m\pi}{b}\right)^2}$

The coefficients d_0 and d_{nm} are given by

$$d_0 = \frac{1}{abk} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} q(x,y) dx dy \tag{7}$$

$$d_{nm} = \begin{cases} 0 & \text{if } n = 0; m = 0 \\ \frac{2}{abkp_{nm}} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} q(x,y) \cos\left(\frac{n\pi(x-0.5a)}{a}\right) dx dy & \text{if } n \neq 0; m = 0 \\ \frac{2}{abkp_{nm}} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} q(x,y) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) dx dy & \text{if } n = 0; m \neq 0 \\ \frac{4}{abkp_{nm}} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} q(x,y) \cos\left(\frac{n\pi(x-0.5a)}{a}\right) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) dx dy & \text{if } n \neq 0; m \neq 0 \end{cases} \tag{8}$$

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = 0 \tag{1}$$

Boundary conditions in x and y directions are

$$\frac{\partial T}{\partial x} = 0 \quad \text{at } x = \pm \frac{a}{2} \tag{2}$$

$$\frac{\partial T}{\partial y} = 0 \quad \text{at } y = \pm \frac{b}{2} \tag{3}$$

Boundary conditions in z direction are

where $p_{nm} = \gamma_{nm} \sinh(\gamma_{nm}c) + \frac{h}{k} \cosh(\gamma_{nm}c)$. Note that the double summation in equation (6) should not include the $n = 0, m = 0$ term since that term has already been included separately.

Problem 2, shown schematically in Fig. 2(b) comprises a known heat flux $q(x,y)$ at the top of a die. The temperature distribution on the bottom face is given as $T_0(x,y)$. Similar to problem 1, in this case, the governing energy equation, and x and y boundary conditions are given by equations (1)–(3) respectively. The z -boundary conditions are given by

$$T(x,y) = T_0(x,y) \quad \text{at } z = c \tag{9}$$

$$\frac{\partial T}{\partial z} = -\frac{1}{k}q(x,y) \text{ at } z = 0 \tag{10}$$

The solution for Problem 2, derived in a manner similar to Problem 1 is

$$T(x,y,z) = d_{A0} + \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} d_{A, nm} \cos\left(\frac{n\pi(x-0.5a)}{a}\right) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) \cosh(\gamma_{nm}z) + d_{B0}(z-c) + \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} d_{B, nm} \cos\left(\frac{n\pi(x-0.5a)}{a}\right) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) \sinh(\gamma_{nm}(z-c)) \tag{11}$$

where $\gamma_{nm} = \sqrt{\left(\frac{n\pi}{a}\right)^2 + \left(\frac{m\pi}{b}\right)^2}$

The coefficients $d_{A,0}$, $d_{B,0}$, $d_{A, nm}$ and $d_{B, nm}$ are given by

$$d_{A,0} = \frac{1}{ab} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} T_0(x,y) dx dy \tag{12}$$

$$d_{B,0} = \frac{1}{abk} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} q(x,y) dx dy \tag{13}$$

where $p_{nm} = \gamma_{nm} \cosh(\gamma_{nm}c)$

Problem 3, shown schematically in Fig. 2(c) has a known heat flux $q(x,y)$ at the top of the die. On the bottom face, the temperature is known to be $T_0(x,y)$ in a region bound by $a_1 \leq x \leq a_2$ and

$b_1 \leq y \leq b_2$, whereas the remainder of the bottom face is adiabatic. Problem 3 is solved by guessing a temperature profile for the adiabatic region on the bottom face, $T_m(x,y)$, so that the temperature profile on the entire bottom face is $T_g(x,y)$ which combines the known field $T_0(x,y)$ with the guessed field in the adiabatic region $T_m(x,y)$. By doing so, problem 3 reduces to problem 2 and the solution is given by equation (11)–(15). Once the temperature field is determined, the outgoing heat flux in the adiabatic region of the bottom face may be computed by the following equation:

$$d_{A, nm} = \begin{cases} 0 & \text{if } n = 0; m = 0 \\ \frac{2}{ab \cosh(\gamma_{nm}c)} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} T_0(x,y) \cos\left(\frac{n\pi(x-0.5a)}{a}\right) dx dy & \text{if } n \neq 0; m = 0 \\ \frac{2}{ab \cosh(\gamma_{nm}c)} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} T_0(x,y) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) dx dy & \text{if } n = 0; m \neq 0 \\ \frac{2}{ab \cosh(\gamma_{nm}c)} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} T_0(x,y) \cos\left(\frac{n\pi(x-0.5a)}{a}\right) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) dx dy & \text{if } n \neq 0; m \neq 0 \end{cases} \tag{14}$$

$$d_{B, nm} = \begin{cases} 0 & \text{if } n = 0; m = 0 \\ \frac{2}{abkp_{nm}} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} q(x,y) \cos\left(\frac{n\pi(x-0.5a)}{a}\right) dx dy & \text{if } n \neq 0; m = 0 \\ \frac{2}{abkp_{nm}} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} q(x,y) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) dx dy & \text{if } n = 0; m \neq 0 \\ \frac{4}{abkp_{nm}} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} q(x,y) \cos\left(\frac{n\pi(x-0.5a)}{a}\right) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) dx dy & \text{if } n \neq 0; m \neq 0 \end{cases} \tag{15}$$

$$Q_{\text{bottom}}(x,y) = k \left(\frac{dT}{dz} \right)_{(z=c)} = k \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} d_{A,nm} \cos\left(\frac{n\pi(x-0.5a)}{a}\right) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) \gamma_{nm} \sinh(\gamma_{nm}c) + kd_{B,0} + k \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} d_{B,nm} \cos\left(\frac{n\pi(x-0.5a)}{a}\right) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) \gamma_{nm} \quad (16)$$

The guessed temperature profile in the adiabatic region on the bottom face is updated as follows:

$$T_{m,\text{new}}(x,y) = (1-w) \cdot T_m(x,y) + w \cdot \left(\frac{Q_{\text{bottom}}(x,y) \cdot c}{k} + T(x,y,z=0) \right) \quad (17)$$

where w is a weighing function between 0 and 1. The weighing function is included to ensure stability of the iterative process. It has been found that values around 0.5 work well for the current problem. $w = 0.5$ has been used for all results presented in this work.

The problem is solved again, and the procedure is repeated until $Q_{\text{bottom}}(x,y)$ is reasonably close to zero in the adiabatic region of the bottom face. This provides the solution to problem 3.

The next sub-section discusses the determination of the temperature field in the N-die stack of unequally sized die using the solutions of the three problems discussed above.

2.2. Solution to the N-die heat transfer problem

The N-die stack comprising of non-uniformly sized die, with heat generation $Q_i(x,y)$ occurring on the device plane of each die is now considered. The first die is assumed to be stacked next to the heat sink, and the Nth die is assumed to be stacked farthest from the heat sink. In order to determine the temperature field for each die, $T_i(x,y,z_i)$ for $-\frac{a_i}{2} \leq x \leq \frac{a_i}{2}$ and $-\frac{b_i}{2} \leq y \leq \frac{b_i}{2}$, each die is considered as a separate domain, and the governing energy conservation equation with appropriate boundary conditions is solved for each die. Continuity of the temperature field and conservation of heat flux at the interface is utilized to derive boundary conditions at the interface between adjacent die. The heat flux entering each die from the top is initially guessed and the guess is iteratively improved until sufficient accuracy is obtained. The procedure is as follows:

- 1 Assume a value for heat fluxes $q_i(x,y)$ entering each die at the top face, $i = 1, 2, \dots, N-1$.
- 2 The heat transfer problem for die1 is identical to problem 1 discussed in section 2.1. $T_1(x,y,z_1)$ is thus determined from equations (6)–(8). As a result, $T_{02}(x,y)$, the interface temperature field between die1 and die2 is computed, since $T_{02}(x,y) = T_1(x,y,z_1=0)$.
- 3 Temperature fields for die 2 through N-1 are computed sequentially. For solving the temperature profile in the i th die, the interface temperature between die i and die $i-1$, $T_{0i}(x,y)$ is computed from the previously determined temperature field of the $(i-1)$ th die and the thermal contact resistance $R_{ci}(x,y)$ between the $(i-1)$ th and i th layers since $T_{0i}(x,y) = T_{i-1}(x,y,z=0) + R_{ci}(x,y) q_{i-1}(x,y)$. As a result, depending on whether the $(i-1)$ th die is larger or smaller than the i th die, the problem of the i th die is identical to problem 2 or problem 3 respectively. Based on the temperature profile $T_i(x,y,z_i)$ computed using section 2.1, the interface temperature between die i and $i+1$, $T_{0,i+1}(x,y)$ is computed and used to compute the temperature profile in the next die. This procedure is repeated until the $(N-1)$ th die.
- 4 For the Nth die, the heat flux entering the top face is known to be $Q_N(x,y)$ and the temperature at the bottom is given by the interface temperature between the Nth and N-1th die, $T_{0N}(x,y)$. In this case, the problem is identical to problem 2 or problem 3 depending on whether the Nth die is smaller or larger than the $(N-1)$ th die.
- 5 Once all temperature fields have been computed, the heat fluxes $q_i(x,y)$ for die $i = 1, 2, 3, \dots, (N-1)$ are computed using energy conservation at the interface between the i th and $(i+1)$ th die as follows:

$$q_i(x,y) = Q^i(x,y) - \delta(x,y) k_{i+1} \left(\frac{\partial T}{\partial z_{i+1}} \right)_{z_{i+1}=c_{i+1}} \quad (18)$$

where $\delta(x,y)$ captures the effect of whether (x,y) , the point on die i under consideration lies within or outside the projection of the $(i+1)$ th die.

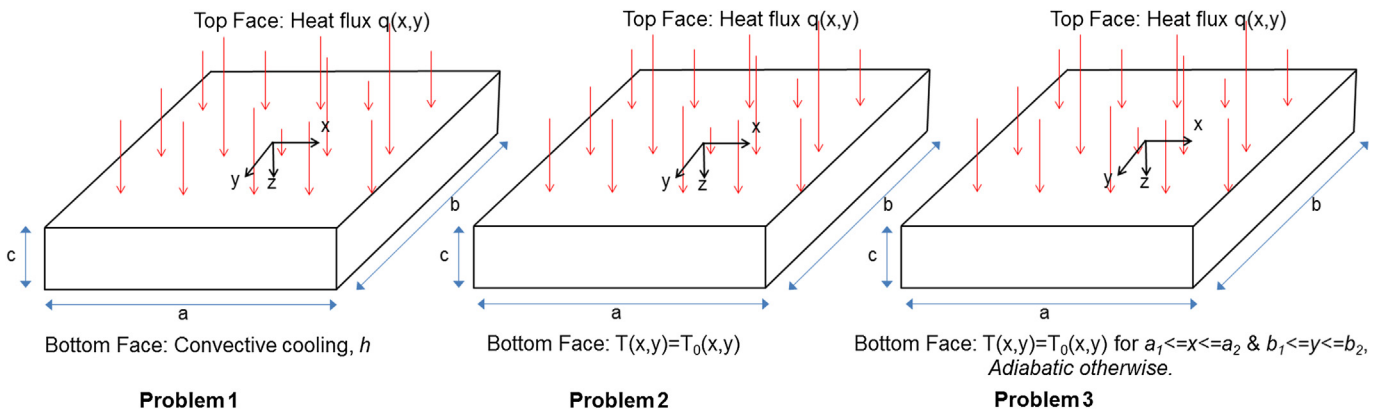


Fig. 2. Schematics of three single-die heat transfer problems solved in Section 2.1. In each case, the four side walls are adiabatic.

$$\delta(x,y) = \begin{cases} 1 & \text{if } \left(-\frac{a_{i+1}}{2} \leq x \leq \frac{a_{i+1}}{2}\right) \text{ and } \left(-\frac{b_{i+1}}{2} \leq y \leq \frac{b_{i+1}}{2}\right) \\ 0 & \text{otherwise} \end{cases}$$

- 6 The heat flux fields $q_i(x,y)$ are updated based on a weighted average of the current and new values.
- 7 Steps 2 through 6 are repeated until the change in the temperature field between successive iterations is sufficiently small.

3. Model results

The analytical model outlined in section 2.2 is used to solve the temperature profile in a multi-die stack with $N = 3$. The three die are assumed to be 8 mm by 8 mm, 10 mm by 10 mm and 4 mm by 4 mm respectively. A single hotspot of size 1 mm by 1 mm and total power of 2.5 W is assumed on each die. The location of the hotspots with respect to the center point of the die is (−1.5 mm, 2.5 mm), (0 mm, 0 mm) and (−1.5 mm, 1.5 mm) respectively. The 8 mm by 8 mm die is assumed to be stacked next to the heat sink, which is modeled with a convective heat transfer coefficient of 5000 W/m²K. This value represents realistic heat transfer coefficients of heat sinks used in the semiconductor industry for typical high-power microprocessor chips. Each die is assumed to be 0.5 mm thick, with a thermal conductivity of 150 W/mK which is representative of Silicon.

Double integrals in equations (7)–(8) and (12)–(15) are evaluated using a two-dimensional Gauss quadrature [38]. Fig. 3 shows the predicted temperature rise at the center of a hotspot as a function of the number of terms included in the double summations in equations (6) and (11). The temperature rise is reported as a fraction of the temperature rise with 1000 terms. It is seen that the predicted temperature value reaches very close to the eventual value, with an error of only 2% using only around 20 terms. Thus, limiting the double summations to only the first 20 terms significantly reduces computation time without affecting accuracy. While Fig. 3 shows the temperature plot for a single die, the trend shown in Fig. 3 has also been verified for a three-die stack. Fig. 4 plots the computed temperature along a line passing through the center of

the hotspot on the second die as a function of the number of iterations employed, following the procedure described in Section 2.2. The solution becomes stable within 5–6 iterations. Beyond the sixth iteration, the difference in the temperature field between successive iterations is less than 0.1%. As a result, the solutions described in this paper are computed using only 7 iterations. This contributes to reduction of computation time without sacrificing quality of results.

Based on the computational simplifications discussed above, the temperature field on a three-die stack described above is computed and compared with finite-element simulations carried out in ANSYS™. Fig. 5 shows the predicted temperature field on the device plane of each of the three die, located at the top of each die. A plot of temperature along lines shown in Fig. 5 is presented in Fig. 6. There is close agreement of the computed temperature fields with finite-element simulations. The temperature rise predicted by the model is within ±4% of finite-element simulation results over the entire temperature field shown in Fig. 5. The agreement improves by increasing the number of terms considered for computing the double integrals in equations (7) and (8) and equations (12) and (15). Figs. 5 and 6 validate the model presented in Sections 2.1 and 2.2.

As further illustration of the model presented above, the temperature field in an unequally-sized three-die stack with a more complicated power map is computed. The power map, shown in Fig. 7 is representative of a typical multi-core microprocessor that combines computing capability with graphics processing. In this case, the four cores are assumed to be distributed in die 2 and 3, whereas the graphics processing unit (GPU) is located in die 1. The temperature map for this floorplan is computed using the model presented in this section, and is shown in Fig. 7. The temperature map clearly shows the influence of the cores that have the highest power density among all heat-generating blocks. In addition, the close proximity of cores with each other, particularly inter-die proximity is also seen to cause an increase in temperature. For minimizing temperature rise, not only do the cores have to be physically separated within each die, but also in adjacent die. This underlines the application of the model presented above to computation of temperature fields in unequally-sized die stacks.

The presence of inter-layer dielectric and bonding materials causes thermal resistance between adjacent die. The analytical model presented in section 2.2 to account for such inter-die

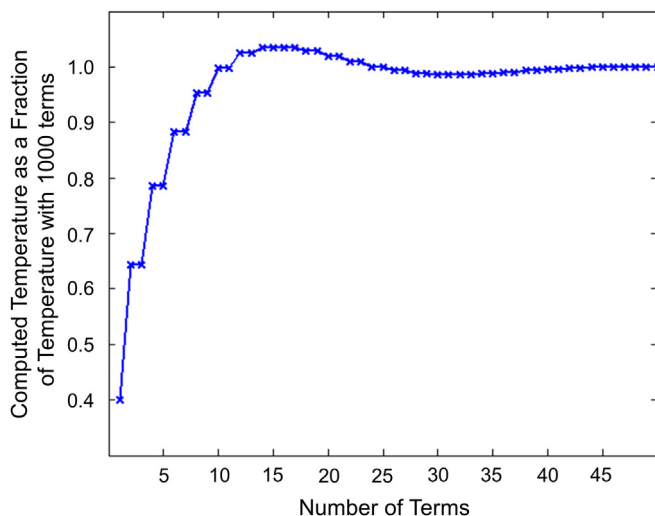


Fig. 3. Effect of the number of terms considered in the double summation on accuracy of temperature computation.

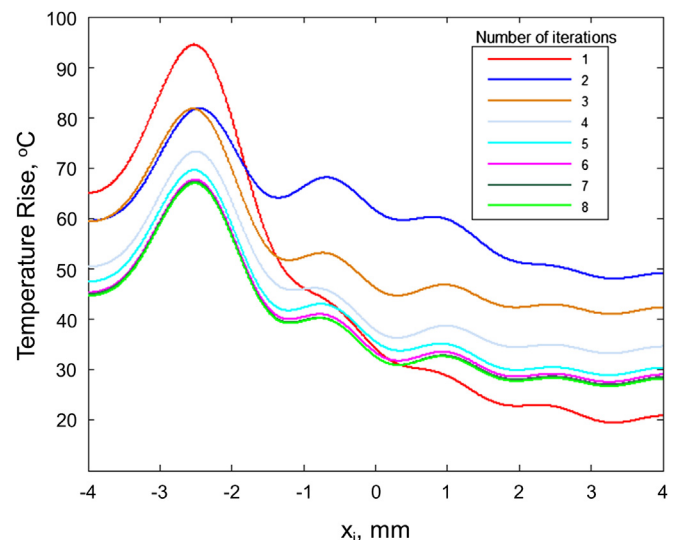


Fig. 4. Effect of the number of iterations on temperature computation accuracy.

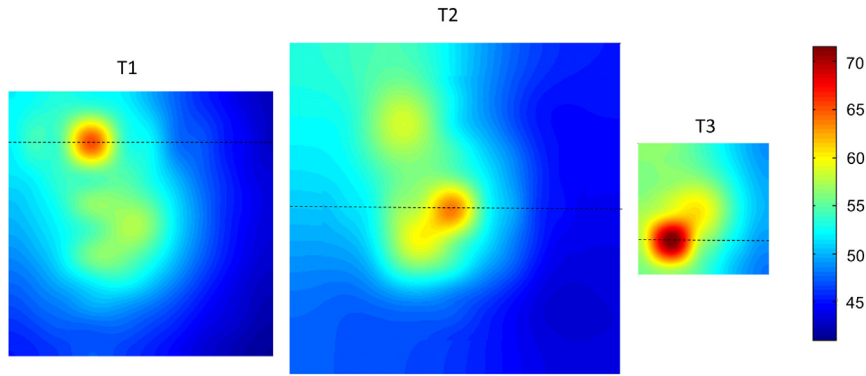


Fig. 5. Temperature field on the device plane of each die in a three-die stack with a hotspot on each die.

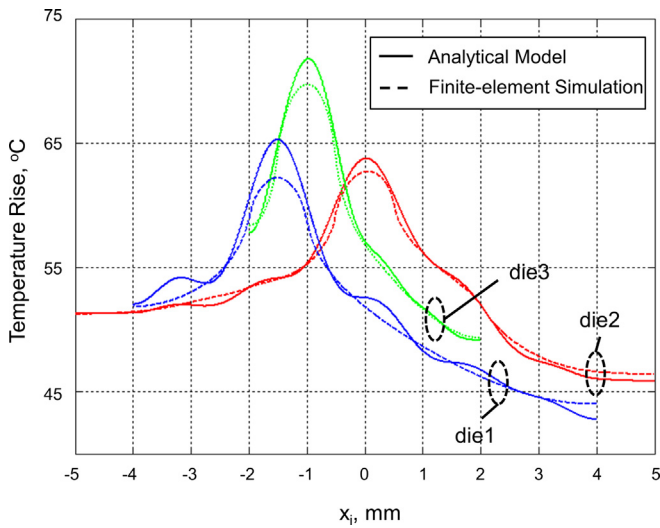


Fig. 6. Comparison of temperature determined from the analytical model with finite-element simulation results along the cross-section lines shown in Fig. 5.

thermal resistances is used to compare the temperature rise in a three-die stack with and without inter-die thermal resistance. Fig. 8 shows the temperature plot along the centerline of die2 for a specific power profile with and without inter-die thermal resistance. As expected, the analytical model predicts a small increase in temperature rise due to the presence of the thermal resistance. The predicted temperature profile is in close agreement with finite-element simulation results. The maximum deviation between the two over the entire die stack is less than 5%, indicating that the model accurately captures the effect of the presence of the thermal resistance. The thermal resistance value of $4 \times 10^{-7} \text{ km}^2/\text{W}$ used in Fig. 8 corresponds to a $10 \mu\text{m}$ thick bond layer with thermal conductivity of 25 W/mK , which are both representative of inter-layer materials in 3D IC technology [25]. Results indicate that for realistic inter-die thermal resistance values, the increase in temperature is small, and is limited to the vicinity of the hotspot.

An alternative way to model the presence of dielectrics, back end-of-line (BEOL) materials and the inter-die bonding layer is to treat each layer as an additional domain with zero heat flux that has the thermal conductivity of the respective material. By doing so, the number of die in the die stack will increase, but the treatment remains the same. Note that since dielectric, BEOL and inter-die bonding layers are typically much thinner than the die itself, it is preferable to treat these layers as a thermal resistance between adjacent die.

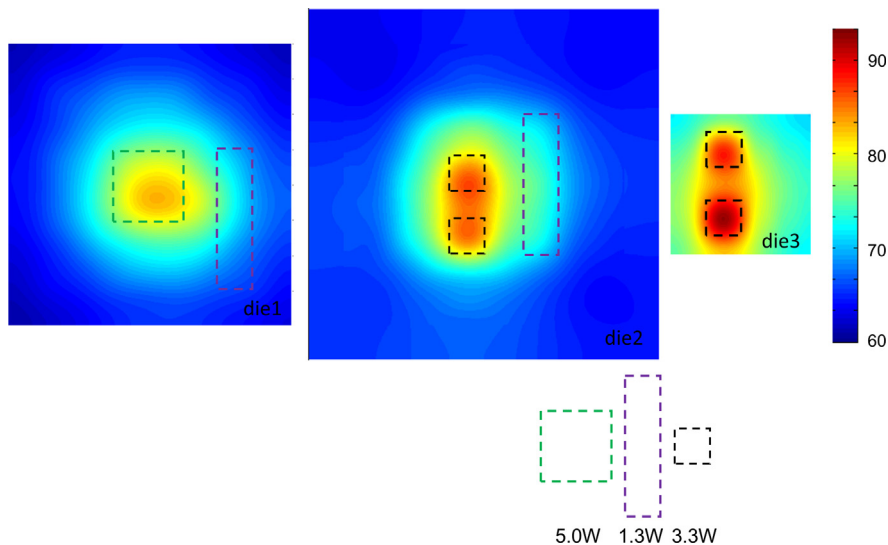


Fig. 7. Computed temperature field in a three-die, unequally-sized stack with non-uniform heating. Power map is shown using hatched lines.

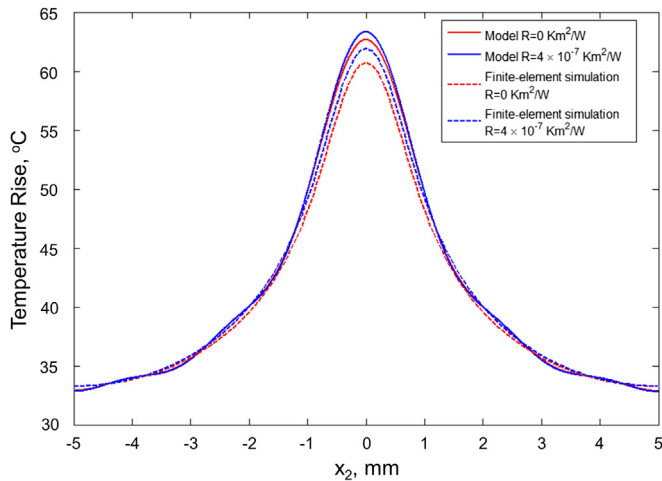


Fig. 8. Temperature plot on die2 for a three-die case with and without inter-die thermal resistance. Analytical model predictions and finite-element simulation results are both shown, and are in close agreement.

4. Application of model for comparison of non-uniformly sized die stack with uniform die stack

Unequally-sized die stacks are motivated primarily by the inherent manufacturing and electrical design benefits. However, it is important to compare the thermal performance of an unequally-sized die stack with an equivalent die stack with uniformly-sized die. In general, changes in the die footprint between adjacent die is likely to cause increased thermal resistance due to heat constriction and spreading [34]. Thus, the larger the degree of non-uniformity, the larger is the expected peak temperature. This is examined quantitatively using the model presented in section 2. Two unequally-sized three-die stacks with varying degree of non-uniformity are compared with an equivalent three-die stack with equally sized die. The equally-sized die is assumed to have die of size 10 mm by 10 mm. The first unequally-sized die stack is assumed to comprise of die of size 11 mm by 11 mm, 10 mm by 10 mm and 9 mm by 9 mm. The second unequally-sized die stack is assumed to comprise of die of size 13 mm by 13 mm, 10 mm by

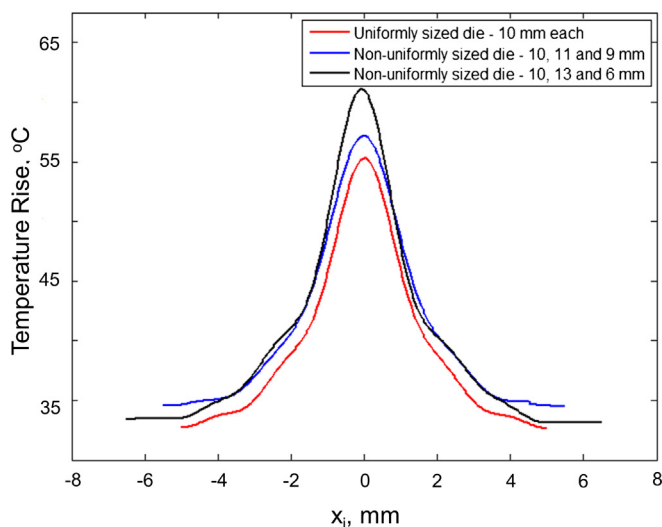


Fig. 9. Comparison of temperature along the centerline of die2 for three cases of three-die stacks with different amounts of die size non-uniformity.

10 mm and 6 mm by 6 mm. The total silicon area is roughly the same in each case. One hotspot of power 3.3 W and size 1 mm by 1 mm is assumed on each die for the three cases considered here. Each hotspot is located at the center of the respective die. Fig. 9 shows the temperature along a line passing through the hotspot on die2 in each of the three cases. Both cases of non-uniform die stacks exhibit higher temperature than the uniform die stack. In addition, the peak temperature is higher for the die stack with the greater degree of non-uniformity in die size. This shows the effect of changes in die size among adjacent die on peak temperature in a die stack. This effect primarily occurs due to additional thermal resistance caused by heat spreading and constriction as heat flows from one die to another.

5. Conclusions

While stacking die with different size in a vertically-integrated 3D IC is attractive from design and manufacturing considerations, doing so introduces additional thermal spreading and constriction resistance in the multi-die stack. The model presented in this work provides an analytical tool for predicting the three-dimensional temperature field in a multi-die stack with an arbitrary number of unequally-sized die. The model shows that the larger the degree of non-uniformity in the die size, the larger is the temperature rise. Tools based on the model presented in this paper may be useful in rapid design iterations and in thermal-electrical optimization of unequally-sized 3D ICs.

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