Interstratum Connection Design Considerations for Cost-Effective 3-D System Integration

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***Abstract*—Emerging 3-D multistrata system integration offers the capability for high density interstratum interconnects that have short lengths and low parasitics. However, 3-D integration is only one way to accomplish system integration and it must compete against established system integration options such as system-on-a-chip (SoC) and system-in-a-package. We discuss multiple tradeoffs that need to be carefully considered for choosing 3-D integration over other integration schemes. The first step toward enabling 3-D design is characterizing the new interstratum connection elements, microconnects and through-Si vias, in a bonded 3-D technology. We have used both analytical- and simulation-based approaches to analyze the parasitic characteristics of interstratum connections between bonded 3-D stratum, and have compared the interstratum power and performance with SoC global interconnects, taking into account the impact of technology scaling. The specific elements in an interstratum connection and their electrical properties strongly depend on the choice of 3-D integration architecture, such as face-to-face, back-to-face, or the presence of redistribution layer for bonding. We present an adaptive interstratum IO circuit technique to drive various types of interstratum connections and thus enable 3-D die reuse across multiple 3-D chips. The 3-D die/intellectual property reuse concept with the adaptive interstratum IO design can be applied to design 3-D ready dice to amortize additional 3-D costs associated with strata design, test, and bonding process.**

***Index Terms*—Microconnect, system-on-a-chip (SoC), 3-D integration, 3-D IO design, through-silicon via (TSV).**

I. Introduction

ACCORDING TO the concepts used for 3-D integration of circuits, multiple device layers exist along the third axis (z-axis), which are connected vertically. This has been accomplished by bonding multiple wafers fabricated with different or similar technologies [1], [9], as well as by fabricating multiple device layers on the same wafer [2] using the epitaxial growth of silicon (Si). In a wafer bonding technology, each device-interconnect layer is fabricated separately on different wafers with the same or different technologies, and then the wafers are bonded with each other using a bonding layer of copper (Cu) or other metals, polymeric adhesives, or oxide-to-oxide bond layers. The bonding technique avoids the issues of forming device quality semiconductor layers over interconnect layers and also has the potential to enhance yield by bonding only known good dice in a die-to-die or die-to-wafer bonding. Hence, 3-D integration via wafer/die-bonding is actively pursued by the industry [1], [3]–[7].

A number of design issues and opportunities arise for 3-D integration. Moreover, 3-D integration is only one way to accomplish system integration and it must compete against established system integration options such as system-on-a-chip (SoC) and system-in-a-package (SiP), as well as the traditional multiple packages on a printed circuit board. In this paper, we will focus on design considerations for the interstratum connections in 3-D. We first provide an overview (Section II) of different 3-D integration options and present a critical comparison of the design tradeoffs associated with the 3-D integration options, SoC, and SiP. Next we present the electrical characterization of new interstratum connection elements, microconnect and through-Si via (TSV), in Sections III and IV using both analytical- and simulation-based approaches. We have analyzed the technology scaling trend of interstratum connections, and compared their power and latency trends with those of SoC global interconnect over various technology nodes. Moreover, we will show that the specific elements in an interstratum connection and their electrical properties strongly depend on and vary with the choice of 3-D integration architecture such as face-to-face, back-to-face, or the presence of redistribution layer for bonding. This complicates interstratum IO circuit design particularly in case of 3-D die reuse, as outlined in Section V. In a general case of cost-effective 3-D system integration, it is desirable to design a die for any one stratum with flexibility to facilitate integration with a number of other circuit dice. One of the major contributions of this work is an adaptive interstratum IO circuit technique, presented in Section V that can accommodate different operating voltages of different strata and varying interstratum parasitic load to enable 3-D die reuse for cost-effective 3-D system integration. Finally, the conclusions of this work are presented in Section VI.

II. 3-D Integration Schemes and System Design Choices

A number of 3-D integration schemes or architectures are available to the system designer. The various 3-D architectures for bonded 3-D integration are based on the key process technologies of: 1) strata thinning and thin strata handling; 2) bonding of strata; 3) formation of through stratum vias or TSVs; and 4) interstratum electrical microconnects, although the order of implementation can vary. The system design objectives interact with the integration scheme selection, which, in

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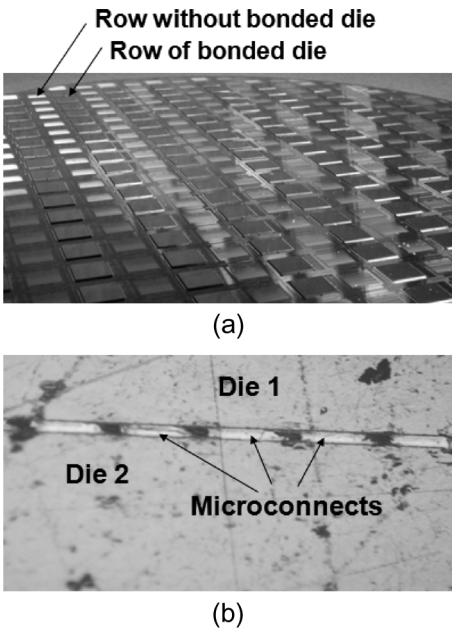

Fig. 1. Die-to-wafer 3-D integration. (a) Die-to-wafer bonded wafer where dice are bonded only on alternative rows of the wafer. (b) Cross section of the metallic microconnect bonded interface for die-to-wafer bond.

turn, interacts with specific details of the process technologies and the resulting 3-D interconnect geometries and parasitics.

A major 3-D bonding architectural choice is between dielectric bonding and metallic bonding. In addition to the differences in bonding materials, this choice also has a substantial impact on the details of the interstratum connections. In dielectric bonding (oxide or polymer bonding), the interstratum connections are completed after bonding by using TSVs to pass through the top die and to connect to the conventional interconnect in the adjacent strata [1], [5]. In metallic bonding, the interstratum connections are completed by bonding pre-existing microconnects [6], and the interstratum connection may include TSVs. Another major option in the bonding of strata is the choice of wafer-to-wafer, die-to-wafer, and die-to-die bonding. Dielectric bonding typically uses wafer-to-wafer bonding, while metallic bonding is commonly associated with any of the three. Fig. 1 shows an example of die-to-wafer 3-D integration with metallic microconnect bonded interface. In this demonstration, dice for the top stratum are bonded only to the alternative rows of dice on the bottom wafer.

Further 3-D bonding architectural choices relate to the relative orientation of the dice in a 3-D stack. The bonding scheme can be face-to-back, face-to-face, or back-to-back, where face refers to the surface on which transistors and the primary interconnect layers are formed and back refers to the Si substrate side of a die. Fig. 2 is a schematic illustration of a 3-D chip with three stacked dice where the bottom two strata are bonded face-to-face and the top two strata are bonded face-to-back. Typical metallic microconnect bonds include interfaces of Cu to Cu, Cu tin alloy, or gold to gold microconnect connections. The microconnects formed on the face of a stratum connect to the last conventional interconnect level of that stratum. Microconnects formed on the back of a stratum connect to the back of TSVs, or in some cases, no separate backside microconnects are formed

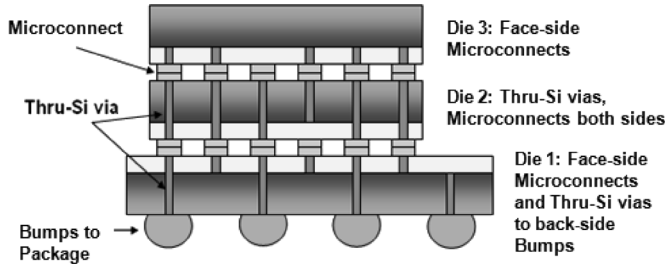

Fig. 2. Schematic illustration of a bonded 3-D chip with three stacked dice.

and the exposed backs of the TSVs are utilized as microconnects. The bonded microconnects provide conductive paths for signal transfer between neighboring dice. The microconnects typically have a pitch in the range from 20 to 60 μm, allowing a high density of interstratum connections. Minimum microconnect pitch is anticipated to further reduce with future development. If microconnects over active devices are allowed then the scaling of the microconnects is only driven by the interstratum interconnect density requirements.

The scaling of TSVs can be a more critical requirement as the TSVs clearly compete for layout space with active devices. As scaling of a TSV footprint is limited by achievable aspect ratio, the substrate may be thinned to a thickness of 100 to 10 μm or even less [7]. The most extreme case of thinning has been achieved with the face-down dielectric bonding of silicon-on-insulator (SOI) with subsequent complete removal of the handle wafer leaving only the thin SOI and buried oxide (BOX) layers [1], [5], [16]. The thinner the substrate, the smaller the practical TSV footprint, but the difficultly of other processes may increase. The effective TSV footprint for layout includes not only the conductive element of the TSV, but also the surrounding dielectric insulation. Additionally, any "keep out" restrictions, which limit proximity of active devices to TSVs, must also be comprehended. Such restrictions could be based on limiting electrical coupling or mechanical stress effects. Depending on the overall 3-D integration architecture, it may be necessary for mechanical strength reasons to have at least one stratum remain reasonably thick. If this stratum has TSVs, then the footprint issues of the resulting larger diameter TSVs can be a greater challenge than for the other strata.

As evident from the above discussion, the major new interconnect elements in a bonded 3-D chip are microconnects and TSVs [8]. In addition to use in interstratum connection, TSVs are also required when electrical signals to the package are connected through backside bumps in a 3-D chip, as illustrated in Fig. 2. An additional design consideration is that metal redistribution layers or an interposer [9] may be needed to obtain the needed connectivity between strata. This especially can be the case for reuse of existing designs in 3-D stacks. The resistive and capacitive loads of such interstratum connections must be considered in the over all 3-D interconnection design.

The choice of a 3-D integration type depends on the specific product application. In addition, 3-D integration is only one way to accomplish system integration. Table I compares major attributes of wafer-to-wafer and die-to-wafer 3-D integration against each other and against SiP and SoC system integrations. The version of the SiP considered in Table I is the case

TABLE I
SYSTEM INTEGRATION CHOICES AND ATTRIBUTES

Attributes	System-in-a-Package (SiP)	3D Wafer-to-wafer	3D Die-to-wafer	System-on-a-Chip (SoC)
SoC–like or better performance	No	Yes	Yes	Yes
Known-good Die Combination	Yes	Limited	Yes	No
Different footprints for different strata	Yes	No	Yes	N/A
Different wafer sizes for different strata	Yes	No	Yes	N/A
Relative form factor	Small	Smallest	Smallest	Moderate
Global interconnect latency	Moderate	Lowest	Lowest	Low
Global interconnect density	Low	High	Medium	High
Differentiated technologies	Yes	Yes	Yes	No
Need for new design tools and technology	No	Yes	Yes	No
Need for new test technology	No	Yes	Yes	No
Thermal management issue	Moderate	High	High	Low

where each stacked die is wire-bonded to the package. There can be a limited number of die-to-die wire-bond connects, but the primary connect is die-to-package [10]. While not listed in Table I, die-to-die integration shares a number of general features with die-to-wafer integration.

One of the key differences between wafer-to-wafer and die-to-wafer is that the former allows parallel bonding of all of the dice on one wafer to all of the dice on the other wafer while die-to-wafer is a serial operation. The serial process is a gating factor for the placement costs of die-to-wafer bonding and frequently results in a tradeoff between placement accuracy and speed. The parallel placement and speed advantage in wafer-to-wafer translates to greater interstratum interconnect densities compared to die-to-wafer. However, the key disadvantages of wafer-to-wafer are: 1) the requirement that the dice on the wafers to be bonded be the same size and 2) the limited ability to pre-select known good die for bonding. As a result, wafer-to-wafer bonding is a more favorable option when wafer yields are high and the die size is small. Stacking multiple copies of the same memory is considered to be advantageous for wafer-to-wafer, as repair can increase the yield and the die are naturally the same size. Die-to-wafer is advantageous for larger die sizes and lower yielding parts. If the stacked strata have differentiated process technologies (say, memory and logic or digital and analog), then the dice may naturally have different sizes and die-to-wafer will be favored.

The ability to integrate differentiated process technologies is one of the major economic advantages of 3-D integration and SiP over SoC. In those cases where differentiated process technologies can be merged into a SoC integration, by the addition of special process steps, the overall process cost will be increased and the yield reduced. A good example is embedded DRAM, where there is a substantial increase in cost to marry the DRAM and logic processes. However, the 3-D stacking of DRAM and logic (microprocessor) allows differentiated functions to be built using optimized processes. Even if the dice to be stacked are all logic, they could still be differentiated by being from different technology nodes. The well-known SoC long wire interconnect latency issue can be effectively addressed in 3-D integration by stacking time-critical blocks and connecting these by short vertical interstratum connections [3]. Therefore, 3-D integration provides power and performance advantages compared to SoC at an additional 3-D process cost that must be taken together with the potential yield enhancement and process differentiation advantages in an overall economics comparison.

In comparison with SiP integration, 3-D integration may be a more expensive option because of previously mentioned key process technologies for bonding. There can be some reduction in form factor, but a more likely driver to move from SiP to 3-D integration will be power and performance requirement related to inter-die interconnects. Inter-die communication in SiP typically has the power and performance disadvantages of off-chip communication. We will show in a later section that 3-D interstratum connections can offer improved power and performance even when compared to on-chip global interconnect over various technology nodes.

For completeness in the comparison, Table I also lists other key attributes such as design complexity, test, and thermal management and how they influence the system integration options. Multiple dice used in SiP are functionally self-contained enabling conventional design tools and test techniques to be used for designing and testing the dice separately. This may not be true for 3-D integration, as designs can be partitioned at a much finer grain (functional unit or even logic gate level) and placed in different strata. Therefore, new design tools and test techniques may be needed for effective 3-D chip design. Thermal management is a concern for SiP and 3-D integrations because both increase the volume density of functional circuit elements. Moreover, the scaling capability of 3-D integration of high-performance chips can substantially increase the power density compared to its SoC counterpart.

III. ELECTRICAL CHARACTERISTICS OF INTERSTRATUM CONNECTIONS

It is essential to adequately model electrical parasitic resistance (R), capacitance (C), and inductance (L) values for interstratum connections and understand their dependencies on key structural properties in order to design the interface circuitry in a 3-D chip and impact 3-D process development for optimum technology-circuit co-design. While there is literature on TSV formation and 3-D bonding processes [11]–[13], published work on electrical characteristics on interstratum connections is still limited [14]–[18]. A majority of the work does not identify the fact that interstratum connection element and electrical characteristics strongly depend on the 3-D bonding schemes. Researchers in [14]–[17] focus only on TSV as the interstratum connection element ignoring the bonded microconnect. which is an essential component in metallic bonding. Moreover, the ef-

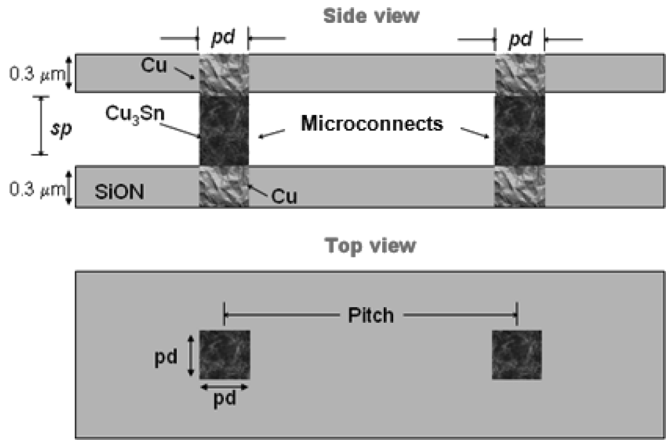

Fig. 3. Bonded microconnect structure for electrostatic simulation.

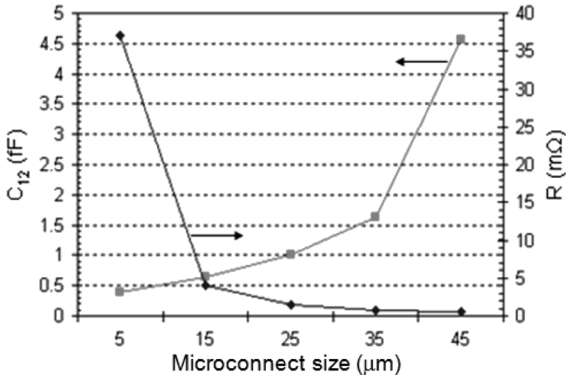

Fig. 4. Microconnect resistance and inter microconnect capacitance versus microconnect size. Here, pitch is 50 μm and $sp = 10$ μm.

fect of sidewall dielectric thickness of a TSV that critically impacts TSV capacitance, as evidenced in Section III-B, is not adequately characterized in [14], [15], [17], and [18]. While some work (e.g.. [15]) focuses on lumped S-parameter extraction and transmission line simulation with TSVs, separated analysis and characterization of *R*'s, *L*'s, and *C*'s of interstratum interconnect elements are more readily useful in 3-D interface circuit design simulations.

In Sections III-A–C, we investigate electrical characteristics and their key dependencies on structural and material properties for both microconnects and TSVs using analytical- and simulation-based approaches. Although parasitic values would vary for different process, geometry, and material choices, our analysis and observation of the variations of electrical parasitics are generally applicable to any microconnects and TSVs. As noted in Section II, these new 3-D interconnect elements generally complete interstratum connections only when used in conjunction with appropriate portions of the conventional interconnection on the strata. As the modeling of the conventional interconnect elements is well established, we will focus on the new 3-D interconnect elements in the following.

A. Microconnect Electrical Characteristics

We have used a 3-D electrostatic simulator [19] to estimate the resistance and coupling capacitance of microconnects. Fig. 3 shows the geometry of a microconnect bonded interface. A microconnect is defined as the complete structure including the bonded material and a portion of the micropad (0.3-μm height) within the passivation dielectric. We use a height sp of 10 μm. Fig. 4 shows inter-microconnect capacitance (C_{12}) and resistance (*R*) for various micropad sizes pd representative of fabricated devices in published literature. For a fixed microconnect pitch of 50 μm, the capacitance is less than 2 fF for micropad dimensions of 35 μm $\times$ 35 μm or less. Resistance of a microconnect decreases with an increase in micropad size pd. The resistance values from our simulation are fairly small with highest value close to 40 mΩ for aggressively scaled microconnects having 5 μm $\times$ 5 μm micropads. A resistivity of approximately 9 $\mu\Omega\cdot$cm is used for Cu_3Sn alloy at the bonded interface.

B. TSV Electrical Characteristics

When an interstratum connection consists of both TSV and microconnect, the TSV tends to be the dominant parasitic component due to its large vertical extension. Neglecting end effects for a cylindrical metal-filled TSV of height of h, radius of $r_{\rm via}$, and dielectric (SiO_2) thickness of t, we can employ the following equations to compute R and C:

$$R = \frac{\rho_m h}{\pi r_{\rm via}^2} \tag{1}$$

$$C = \frac{2\pi\varepsilon_r\varepsilon_o h}{\ln\left((r_{\rm via}+t)/r_{\rm via}\right)} \tag{2}$$

where $\rho_{\rm m}$ is the resistivity of TSV conductor, and ε_r and ε_o are relative permittivity of SiO_2 and permittivity of empty space, respectively. The above equations indicate that resistance inversely scales with $r_{\rm via}^2$, while capacitance inversely scales with $\ln$ (ratio of radii) for a fixed h. We will consider Cu-filled TSVs in this work for their low electrical resistivity. For a 50-μm-long cylindrical TSV of 5-μm diameter and 1-μm sidewall dielectric thickness, capacitive and resistive loads are 0.04 pF and 43 mΩ, respectively. Equation (2) assumes that the inner and outer electrodes are both good metals. Since the outer electrode is Si, this approximation will breakdown for lower doped substrates and higher frequencies, but in any case, it will provide a conservative or maximum capacitance estimate.

Consider the coupling between two TSVs spaced at a pitch p. A simplified lumped element equivalent circuit could be considered to be the parallel combination of the Si resistance $R_{\rm Si}$ and Si capacitance $C_{\rm Si}$, which is then in series with the capacitances of the two TSV sidewall dielectrics. The impedance of the Si is given by

$$Z_{\rm Si} = R_{\rm Si}/(1 + j2\pi f C_{\rm Si} R_{\rm Si}) \tag{3}$$

where f is the frequency. The overall impedance Z_{12} between the two TSVs is given by

$$Z_{12} = 2Z_{TSV} + Z_{\rm Si}. \tag{4}$$

The inter-TSV capacitance C_{12} is related to the impedance of the above equivalent circuit according to

$$C_{12} = -1/2\pi f \mathrm{Im}(Z_{12}). \tag{5}$$

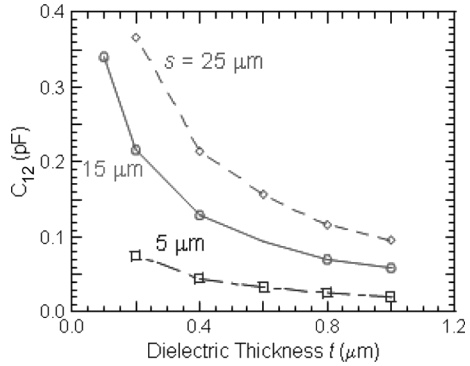

Fig. 5. Inter-TSV capacitance as a function of sidewall dielectric thickness and via dimension. Here, via pitch is 30 μm, Si resistivity is 10 $\Omega \cdot$ cm, and signal frequency is 100 MHz.

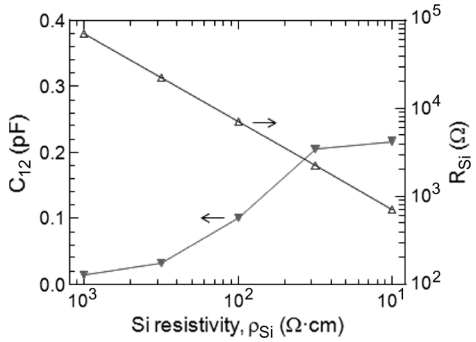

Fig. 6. Inter-TSV capacitance (C_{12}) and Si resistance $(R_{\rm Si})$ as a function of Si resistivity $(\rho_{\rm Si})$ for the case of $f = 100$ MHz, dimension $s = 15$ μm, pitch $p = 30$ μm, dielectric thickness $= 0.2$ μm, and TSV height of 50 μm.

From (3), it is seen that at lower frequencies and lower Si resistance, the Si impedance can be approximated by the Si resistance, and the capacitance C_{12} approaches the series capacitance of the two TSVs. However, at high frequencies and higher Si resistance, the Si impedance can be approximated by the Si capacitance, and the capacitance C_{12} approaches the series capacitance of the two TSVs and Si capacitance. The Si capacitance will be small compared to TSV sidewall dielectric capacitances for realistic geometries as considered here, and hence, the capacitance C_{12} decreases at high frequencies.

A more accurate estimate of the coupling capacitance between two TSVs is obtained by using 2-D electromagnetic simulations to investigate the relationship of capacitance with signal frequency and Si resistivity. The simulated geometry consists of two square TSVs with a pitch of p, and each square via with a side dimension of s, dielectric thickness of t, and a height of $h = 50$ μm. Due to the relatively deep TSVs, 2-D simulation can sufficiently model the dominant coupling path and end-effects can be ignored. Fig. 5 shows inter-TSV capacitance C_{12} as a function of dielectric thickness and TSV dimension for the case of $p = 30$ μm, $\rho_{\rm Si} = 10\,\Omega \cdot$ cm, and $f = 100$ MHz. For this situation, the low Si resistivity and the low frequency allow the Si between the two TSV conductors to act as a metal.

Now consider the situation where the resistivity of the Si is allowed to increase. In the limit of high Si resistivity, the Si acts as a dielectric, and the inter-TSV capacitance (C_{12}) is effectively formed by the series combination of the TSV sidewall dielectric liners and the Si capacitance. As a result, C_{12} saturates at a low value. Fig. 6 shows C_{12} and Si resistance as a function of Si resistivity for a pair of TSVs with a pitch of 30 μm, dimensions of 15 μm, dielectric thickness of 0.2 μm, and height of 50 μm.

The simulation results in Figs. 5 and 6 correspond to a signal operation frequency of 100 MHz through a TSV. While the inter-TSV resistance $(R_{\rm Si})$ due to the Si substrate is independent of signal frequency, the inter-TSV capacitance (C_{12}) decreases with higher signal frequency, as illustrated in Fig. 7. The results suggest that accurate modeling for TSV capacitance needs to account for the interstratum connection bandwidth desired in a 3-D system. Equation (2) and simulation results obtained for low signal frequency and low resistivity can provide for conservatively high estimates of inter-TSV capacitance.

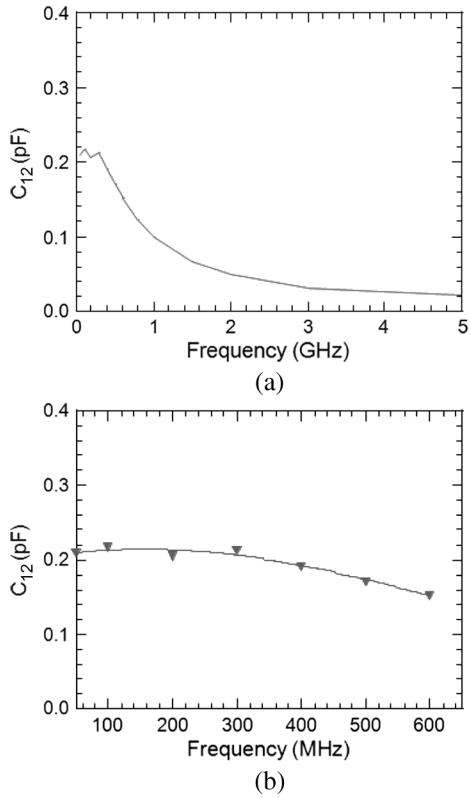

Fig. 7. Inter-TSV capacitance (C_{12}) as a function of signal operating frequency for: (a) a wider range of frequencies and (b) expanded lower frequency results. Here, TSV size $s = 15$ μm, sidewall dielectric thickness $t = 0.2$ μm, TSV pitch $p = 30$ μm, height $h = 50$ μm, and Si resistivity $\rho_{\rm Si} = 10\,\Omega \cdot$ cm.

Inductance characterization is much more complex, as it is essential to include a return path, which is directly related to the design and layout of specific interface circuitry. In various simulation scenarios of two TSVs in a substrate at varying pitch, we estimated a maximum inductance of 0.9 pH/μm (of TSV height) when TSVs are at 100-μm pitch and one serves as the return path. Inductance would be lowered when return paths are present at closer spacing. Simulation studies in [18] report approximately a 0.3-pH/μm inductance for their 30-μm-pitch and 15-μm-diameter TSVs. Similarly, measured inductance in [14] using a two-port TSV test structure where the return path is within 70 μm is reported to be less than 0.4 pH/μm for a via aspect ratio of 10 : 1 or lower. Therefore, TSV inductance is expected

TABLE II
INTERSTRATUM CONNECTION ELEMENTS AND PARASITIC LOADS

Element	Critical Dimensions	Parasitics
Microconnect	Footprint: 5 μm x 5 μm	R = 40 mΩ
		C = 0.4 fF
Through-Si Via	Footprint: 5 μm x 5 μm	R = 43 mΩ
	Sidewall thickness, t: 1 μm	C = 40 fF
	Height, h: 50 μm	

to be very low. When the inductance is from 10 to 50 pH and the capacitance is in tenths of a picofarad, the resonant frequency $(f_o = 1/2\pi\sqrt{(LC)})$ is in the order of 100 GHz. For signal operating frequencies significantly smaller than the resonant frequency, such as in the few gigahertz range, the capacitance and resistance dominate the overall impedance of the TSV. Thus, as long as reasonable return paths are provided, the inductance values can be ignored in the range of 1 GHz and below, as is done in the remainder of this study. As the inductances would impact the performance of a power distribution network, further studies are required for the effect of inductance on the power distribution network with interstratum connections.

The above analysis, as well as the analysis in following sections, is most appropriate for the case of metallic bonding where the TSVs are typically fabricated primarily within the Si substrate. For the case of dielectric bonding, the situation can be more complicated. The TSVs from top stratum to the bottom stratum must pass through the complete conventional multilevel interconnect stack of the top stratum. Thus, the capacitance calculations will need to be modified, and the overall electrical characteristics would also be different for such interstratum vias as can be found in [16]. For dielectric bonding, if the Si substrate is less aggressively thinned, for example, to a thickness of approximately 50 μm, as considered in our analysis, then the TSV capacitance is still dominated by the portion within the substrate Si. However, if the Si substrate is more aggressively thinned, then the portion of the TSV within the conventional interconnect becomes a more important factor, and if the substrate is SOI, the portion of the TSV within the BOX layer may also need to be considered in the capacitance calculation. In the extreme case of thinning an SOI substrate to the BOX layer, as illustrated in [1] and [5], the TSVs will primarily be within the multilevel metal stack and very little within the thin SOI layer. Thus, an analysis of TSV parasitics appropriate for that geometry should be utilized.

C. Interstratum Geometry Choice for Interface Design

A practical TSV aspect ratio of 10 : 1 or lower is used, as this is within current process capability. The overall TSV dimensions are limited by strata thinning and thin strata handling process capability. For example, a substrate thinned down to 50 μm would limit a TSV footprint to 5 μm $\times$ 5 μm or larger. To further complicate the aspect ratio and TSV size interaction, our study in Fig. 5 indicates that the sidewall dielectric thickness needs to be high, such as 1 μm, to reduce parasitic capacitance of a TSV. Table II shows the microconnect and TSV dimensions and corresponding *RC* values to be used in the remainder of this interface circuitry design study.

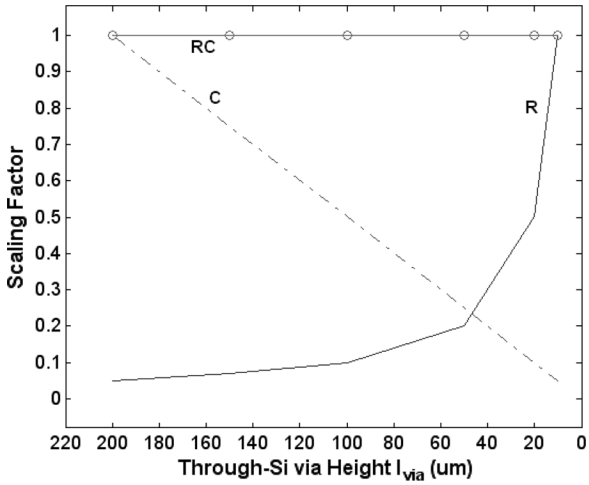

Fig. 8. Parasitic resistance and capacitance scaling trend of a TSV.

Comparing these *R* and *C* values to other published studies, researchers in [18] reported approximately 20-mΩ resistance for 15 μm diameter $\times$ 125 μm long TSVs and approximately 200-fF capacitance for 25 μm diameter $\times$ 150 μm long TSVs. Researchers in [14] reported approximately 60-mΩ resistance and 270–310-fF capacitance for 10 μm diameter $\times$ 100 μm long TSVs. The choice and variations in critical dimension parameters, such as footprint, via height, and sidewall thickness lead to the differences in TSV parasitics.

IV. INTERSTRATUM CONNECTION SCALING AND LATENCY/POWER TREND

Assuming a constant TSV aspect ratio and constant ratio of radii in (2), we investigated the impact of TSV height (h) or equivalently the effect of substrate thinning. In this case, TSV radius $r_{\rm via}$ and sidewall thickness t scale linearly with via height. As illustrated in Fig. 8, resulting *R* and *C* scale inversely with respect to each other while the *RC* product remains unchanged (ignoring current crowding or scattering effects at the smaller dimensions) with substrate thinning. As technology nodes continue to scale, a smaller TSV footprint in a thinner substrate would allow higher densities of interstratum connections while the *RC* product in the first order remains unchanged.

Multiple studies in the past have illustrated the interconnect performance improvement in 3-D integration by comparing the on-chip wire length distribution of 2-D and 3-D chips [2], [20], [21]. A significant number of long global wires can be replaced by interstratum connections in 3-D integration where functional blocks are stacked and connected vertically. Therefore, it is important to relate interstratum connection *RC* delay and power with those of global interconnect, and investigate the effect due to technology scaling.

A long global interconnect is optimally buffered by inserting properly sized repeaters or drivers at smaller interconnect segments or stages. Researchers in [20] investigated global interconnect delay in 2-D and 3-D integrated circuits (ICs) using an analytical approach for modeling interconnect and gate delay. Using the same analytical method as in [20] and applying it to the most recent International Technology Roadmap of Semiconductors (ITRS) data, we estimated delay per 1-mm-long global wire

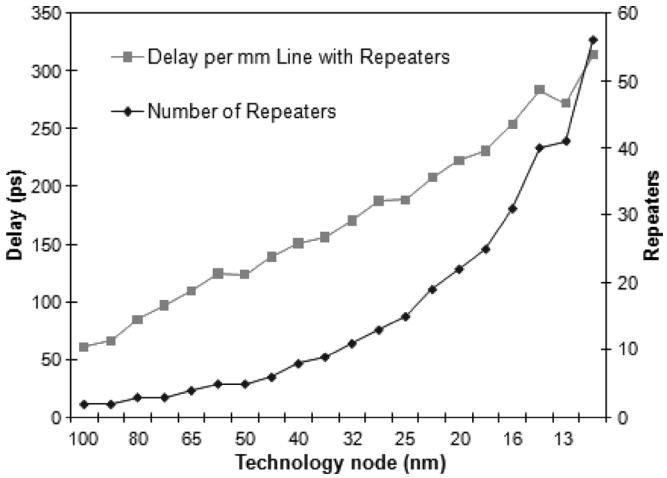

Fig. 9. Global interconnection delay per millimeter length with repeaters, and the number of repeaters per millimeter of global interconnect length.

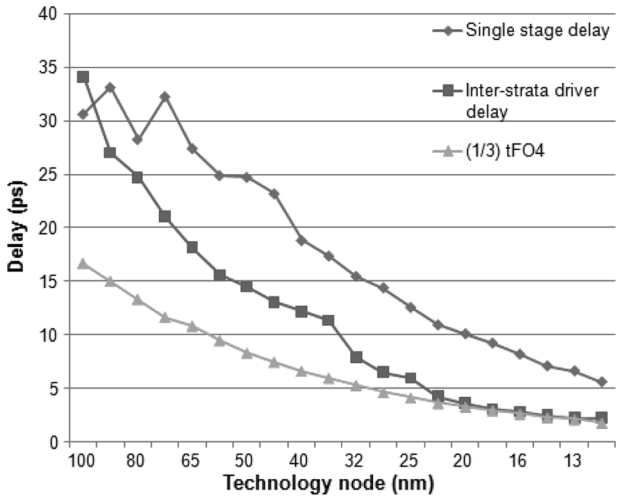

Fig. 10. Interstratum driver delay comparison with single stage delay in global interconnect and fan out of four (FO4) gate delay.

with optimally placed repeaters and the number of repeaters, as illustrated in Fig. 9. The 100–70-nm node parameters were extracted from ITRS 2004 and 2006 reports, while 65 nm and below parameters are from the ITRS 2007 report [22].

The global wire delay per millimeter of length increases linearly with the technology node when repeaters are inserted at the scaled critical length. However, each technology node adds the expense of a significantly increasing number of repeaters. Using data from Fig. 9, we can estimate single-stage repeater delay, measured from the input of an inverter/repeater to the input of the next inverter/repeater for each technology node. Fig. 10 shows technology node scale plots of the single stage repeater delay and the interstratum connection driver delay, which is obtained from SPICE simulation of an optimally sized inverter in 90-nm technology driving a 5 μm $\times$ 5 μm TSV with a microconnect, as shown in Table II, and then scaled accordingly to estimate delay for each technology node. Using a signal transmission frequency of 800 MHz and Vdd supply voltages from the ITRS, we also estimated power consumption of an interstratum driver and compared this with the power consumptions of a 1-mm-long global wire and a single-stage repeater

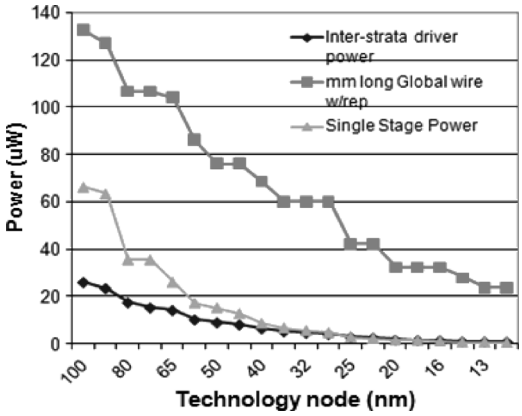

Fig. 11. Interstratum driver power comparison with global interconnection.

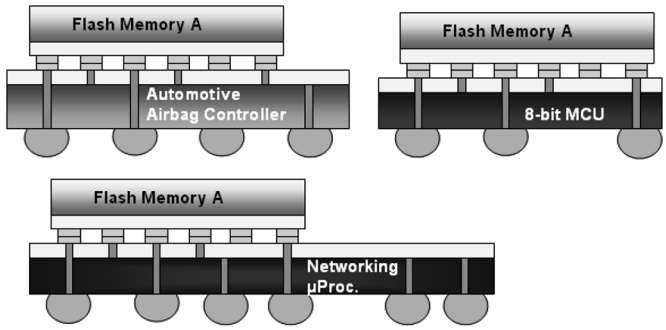

Fig. 12. Schematic illustration of 3-D die design reuse.

in each technology node, as illustrated in Fig. 11. Interestingly, interstratum signal transmission power is significantly smaller than total power in a 1-mm-long global wire with repeaters and is comparable to single stage power in the global wire.

Smaller interstratum connection driver delay compared to even a single-stage delay of a global wire confirms that interstratum connections can be effectively utilized to increase performance with reduced power for global routing in a 3-D chip compared to its 2-D counterpart. Fig. 10 also plots one-third of a gate delay with a fan-out of four (t_{FO4}) for comparing our interstratum connection delay with that of [23] where a die-to-die via delay is calculated using SPICE simulation for a 70-nm technology node. The die-to-die via in [23], which is formed using face-to-face bonding, and is more a microconnect than a TSV. As a result, our estimated interstratum connection delay with microconnect and TSV is an average of 1.5$\times$ longer than the die-to-die via approximated delay of one-third of t_{FO4}.

V. Interstratum IO Design for 3-D Die Reuse

We have seen how parasitic load can significantly vary depending on the interstratum connection elements, such as microconnects and/or TSVs, and their critical dimensions in Section III. In addition to bonding schemes, parasitic load would vary due to loading from any added interposer die or a redistribution layer. This complicates interstratum IO circuit design particularly in the case of die reuse in 3-D integration.

The concept of 3-D stackable design that comprehends die reuse is illustrated in Fig. 12. Here, the same flash memory die

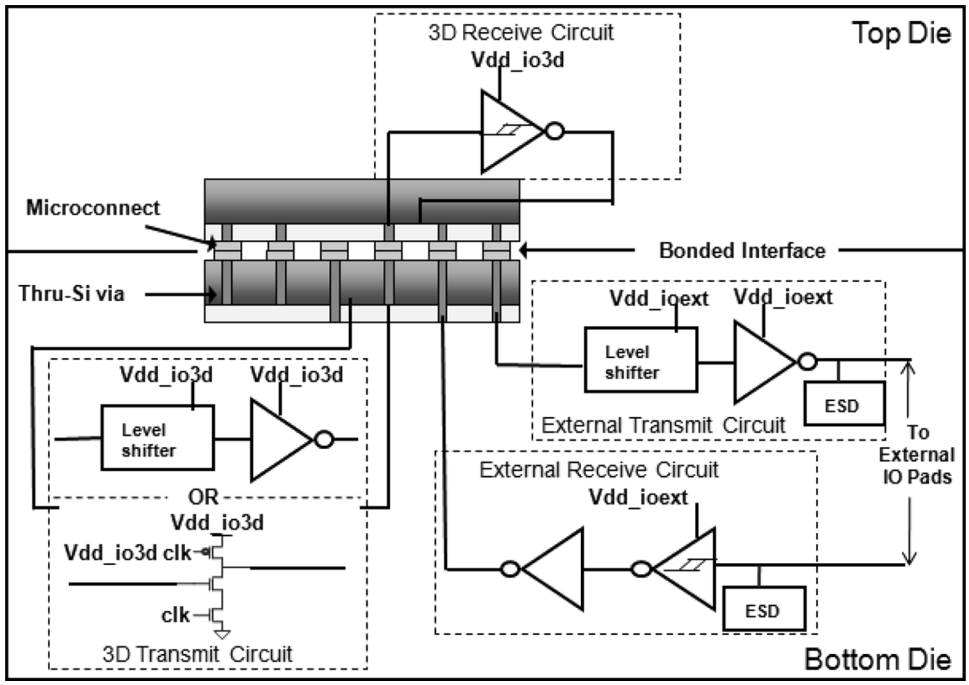

Fig. 13. Schematic illustration of the proposed 3-D interstratum IO technique. Standard external IO in the 3-D chip is also shown.

for top stratum is used in three different 3-D chips with a microprocessor or microcontroller die in the other stratum. While this concept has not yet been implemented in 3-D integration, there are a number of apparent advantages in 3-D die reuse. Being able to reuse a 3-D die across multiple products would increase the cost effectiveness of 3-D integration in multiple ways. In addition to reduced design time due to true intellectual property (IP) reuse and mask cost reduction, the IP in any one stratum could be on different technology nodes. For example, flash memory A in Fig. 12 could be retained at a given technology node, while another stratum, where scaling is the key to performance improvement, e.g. the microprocessor, scales to the latest technology node. Thus, designed-in 3-D die reuse would allow avoiding noncritical technology migration for reduced time-to-market and significant cost reduction.

Despite several challenges, new design techniques can enable 3-D die reuse. The issue of varying die sizes for different strata can be managed by using die-to-wafer bonding, as discussed in Section II. To address the issue of achieving connectivity between dice, which were not designed to a common interface, either an interposer die or preferably a redistribution layer with metal routing can be employed to provide the required connectivity. To avoid the need for a redistribution layer or an interposer die, 3-D interface standards can be developed to allow die reuse and encourage wider use of 3-D IPs such as the physical standard of interface characteristics for memory stratum recently proposed in [24]. A third issue associated with 3-D interstratum IO design is related to accommodating varying operating voltages of the different strata, interstratum connection parasitics, and power requirements across different 3-D chips. We present an adaptive 3-D interface circuit technique that enables robust signal transfer through various types of interstratum connections using the same interface circuitry.

Fig. 13 shows a schematic illustration of the general concept in the proposed technique. The circuit for receiving a signal from an interstratum connection includes a hysteresis buffer where the input stage has an isolated power supply connection (Vdd_{io3d}) for independent control. Similarly, the circuit for transmitting a signal through an interstratum connection consists of a level shifter and output driver with isolated power supply connection (Vdd_{io3d}) for independent control as well. The level shifter and driver stages can alternatively be combined with dynamic circuit design style, as shown in the Fig. 13, to reduce the transmit circuit delay using a clocked interface. In a bonded 3-D chip, the isolated power supply connections from both receiver and transmitter circuits are connected with each other and controlled via a common external pin which would set a common voltage for interstratum signals. A 3-D specific die or stratum could be designed to allow Vdd_{io3d} to be set at different levels depending on the type of interstratum connections and what die is used in the other strata. The level of Vdd_{io3d} could be set by supplying an external voltage at this value. Alternatively, the level of Vdd_{io3d} could be set by negotiation between the various strata, e.g., Vdd_{io3d} could be set to the highest internal bus voltage amongst the dice.

Some similarities can be drawn between the proposed interstratum IO design scheme and the voltage island technique commonly used in conventional designs where individual circuit blocks, such as a core or memory, can be operating at a different voltage supply than rest of the chip. In many applications, voltage islands are designed for low power consumption, power management, and performance optimization [25], [26]. According to the proposed interstratum IO design scheme, the interface circuitry in 3-D can be contemplated as an interface block on its own voltage island that has a different Vdd supply from rest of the circuitry in neighboring strata. However, in con-

ventional voltage island technique, design factors such as the supply voltage of an island and interface to circuits on other voltage domains, are determined and optimized during design time. On the contrary, different operating voltages of the different strata and varying interstratum connection parasitics with bonding schemes cannot be fully deterministic in case of 3-D die reuse during design of any one stratum. Therefore, the adaptive 3-D interstratum IO technique is proposed to address the above uncertainties post-Si using the Vdd supply controllability.

A. 3-D Interstratum IO Design Case Study

We report a case study where a 3-D die is first designed for a microconnect only bonded interface, and then where the design is reused in different bonding schemes that include TSVs and a redistribution layer. We consider the following three interstratum IO circuitry implementation choices.

1) *Custom 3D-Buffer (C-3DBuf)*: As presented in [27], the Custom 3D Buffer scheme (C-3DBuf) consists of a single inverter at the transmit side and a single inverter at the receive side with a fixed supply voltage ($Vdd = 1.0$ V used in our study). Here, the transmit inverter is sized x to optimally drive a 5 μm$\times$5 μm microconnect, as in Table II, and the receive inverter is sized y. The receiver y is $0.25x$ in size.
2) *Adaptive 3DIO (A-3DIO)*: This is our proposed IO circuit technique with externally selectable supply voltage and hysteresis at the receive inverter. The transmit inverter is sized x similar to above C-3DBuf and the receive inverter is sized approximately 1.8 y due to the two added transistors for hysteresis.
3) *Standard External IO (SEIO)*: This is a standard external IO circuit scheme (SEIO) that might be available as a hard macro from a library, designed to drive approximately a 40-pF load with maximum 2-V/ns slope with a fixed power supply $Vdd\_\mathrm{ioext} = 2.0$ V. The corresponding transmit inverter size, for comparison with C-3DBuf and A-3DIO, is approximately $5x$ and receive inverter size is 1.8 y. We will not consider additional area penalty in SEIO associated with electrostatic discharge (ESD) protection. In this study, we will compare the area of transmit and receive inverters.

B. Simulation Results

The above three interstratum IO circuitry schemes are simulated for delay and power consumption with three different cases of interstratum connections. The microconnect and TSV dimensions are as mentioned in Table II. The results from the design case study are reported in Table III. Table III first reports interstratum signal delay (measured from the input of the transmit inverter to the output of the receive inverter) and power consumption simulated using a 90-nm CMOS technology for case (a), a microconnect-only bonded interface. We assume that the maximum allowable interstratum signal delay for the 3-D chip is 200 ps for a positive timing slack along the path. The interstratum signal frequency is 500 MHz in this design case study. All three designs meet the delay requirement for case (a) with C-3DBuf having the lowest delay for similar power consumption as A-3DIO. It is important to note that SEIO does not enable smaller delay than others due to self-loading from source/drain capacitance at the bonded interface. While the above SEIO design can be used in this case, the general idea of using standard external IO circuitry for 3-D interstratum IO is, however, not applicable to all design scenarios because of excess self-loading and interstratum signal delay.

TABLE III
INTERSTRATUM IO DESIGN COMPARISON

Case	IO Scheme			Metrics	
	Name	Vdd (V)	Nom. Gate area	Delay (ps)	Power (μW)
(a) Microconnect only	A-3DIO	1.0	.27	152	57
	C-3DBuf	1.0	.23	113	50
	SEIO	2.0	1	191	4116
(b) Microconnect + thru Si via	A-3DIO	1.0	.27	174	75
	C-3DBuf	1.0	.23	136	68
	SEIO	2.0	1	195	4152
(c) Microconnect + thru Si via + 0.5 mm re-distribution routing	A-3DIO	1.0	.27	277	224
	A-3DIO	2.0	.27	199	1356
	C-3DBuf	1.0	.23	218	216
	SEIO	2.0	1	227	4536

Table III next reports delay and power data when the 3-D dice with the three different interstratum IO circuitry are reused in bonding schemes for the cases where (b) an interstratum connection consists of a microconnect plus TSV and (c) microconnect plus TSV plus 0.5-mm metal routing for a redistribution layer. The additional resistive and capacitive loads due to metal routing in the redistribution layer are 3.3 Ω and 300 fF, respectively, which is a representative load for a 3-μm wide, 0.5-mm long global wire in 90-nm technology.

All three interstratum IO designs meet the performance requirement in case (b). The C-3DBuf scheme performs best in both delay and power while the SEIO scheme performs worst with longer delay and as much as two orders of magnitude higher power consumption. In case (c), on the other hand, none of the designs, C-3DBuf, SEIO, and A-3DIO with 1.0-V supply, initially meet the delay requirement of 200 ps due to additional redistribution layer loading. To meet the timing requirement in this case, we can externally set A-3DIO's power supply to 2.0 V and enable die reuse at the same performance. The configurability in the proposed A-3DIO scheme allows us to use the same design optimally by scaling Vdd, and thus, enabling 3-D die reuse in case of various bonding scenarios. While we use only 0.5-mm metal routing for the redistribution layer in this case study, longer routing in a redistribution layer or in an interposer die would contribute to even larger parasitic loads for which Vdd configurability alone may not be sufficient to meet the performance goal. In such cases, additional configurability using methods, such as variable driver strength and/or optionally adding repeaters for long redistribution routing, would be desirable in an adaptive 3-D IO design scheme.

In addition to the configurability to meet a performance goal with lower power consumption in various bonding scenarios, another obvious 3-D die reuse scenario where our proposed technique is required is when the other die uses a different operating voltage. The slightly worse area and delay metrics of

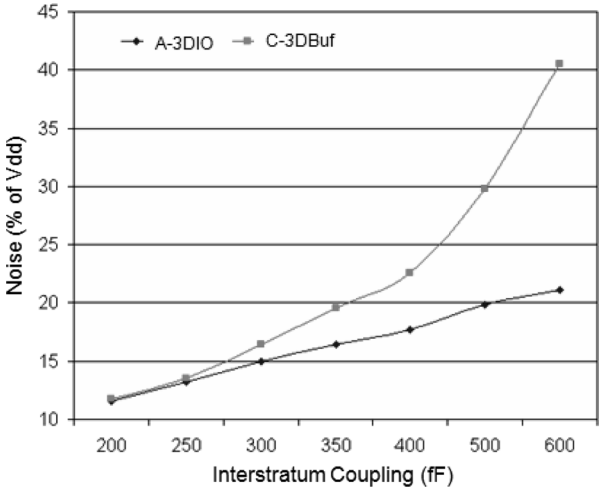

Fig. 14. Interstratum signal coupling noise as a function of interstratum coupling capacitance at the victim signal's receiver output.

A-3DIO over C-3DBuf are due to the hysteresis transistors in the receive inverters. However, the hysteresis inverter provides enhanced interstratum signal coupling noise immunity, as illustrated in Fig. 14, and would be essential particularly for interstratum connections consisting of TSVs and a redistribution layer or an interposer die where the capacitive coupling between two interstratum signals can be high. Thus, the design approach in A-3DIO is well suited for design scenarios where interstratum connection loads and interstratum connection operating voltages are not fully deterministic during the design, allowing a 3-D die to be reused for integration with multiple other 3-D dice.

VI. Conclusion

The new elements in an interstratum connection, i.e., microconnect and TSV, depend on the choice of 3-D bonding scheme such as face-to-face or face-to-back bonding. As a result, the electrical parasitics of interstratum connections vary with different bonding schemes and the presence of any redistribution layer or interposer die for bonding. We have analyzed the electrical characteristics of microconnects and TSVs to understand the correlation between parasitics and key structural and material properties. We also presented a technology scaling trend of interstratum connections, and compared their power and latency trends with those of the SoC global interconnect over various technology nodes. Based on our parasitic estimation of an interstratum connection, we show that the interstratum connection driver latency is smaller than even a single-stage global wire latency with less or comparable power consumption across various technology nodes. Thus, 3-D integration has the potential for SoC like or better performance with the added capability of differentiated technology integration like SiP integration. The varying parasitics of interstratum connection with bonding schemes and different operating voltages due to differentiated technology integration complicate the interstratum IO circuitry design particularly for 3-D die reuse. We presented an adaptive interstratum IO circuit technique (A-3DIO) to enable 3-D die reuse across multiple 3-D chips for cost-effective 3-D system integration. A design case study comparing A-3DIO with custom 3DIO design and standard external IO circuitry demonstrates that the design approach in A-3DIO is more power efficient and well suited to meet performance requirements for design scenarios where interstratum connection loads and operating voltages are not fully deterministic during the design. The 3-D die/IP reuse concept with the adaptive 3DIO design can be applied to design 3-D ready dice to amortize additional 3-D costs associated with the strata design, test, and 3-D process.

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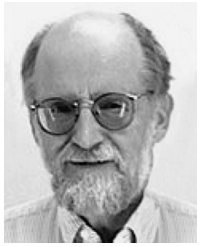

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